|| Jai Sri Gurudev ||

Sri Adichunchanagiri Shikshana Trust[R]

SJC INSTITUTE OF TECHNOLOGY

CHICKBALLAPUR – 562101

DEPARTMENT OF

ELECTRONICS & COMMUNICATION ENGINEERING

ANALOG AND DIGITAL ELECTRONICS LAB MANUAL (21ECL35)

III SEMESTER

PREPARED BY

NIRMALA DEVI A C

Dr. NAGENDRA KUMAR M

J B KALAIAH

VISHALA I L

REVIEWED & APPROVED BY

Dr. B N SHOBHA

HOD

Dept. of ECE

SJCIT

SJC INSTITUTE OF TECHNOLOGY

VISION

Preparing Competent Engineering and Management Professionals to Serve the Society.

MISSION

- **Providing Students with a Sound Knowledge in Fundamentals of their branch of Study.**
- **Promoting Excellence in Teaching, Training, Research and Consultancy.**
- **Exposing Students to Emerging Frontiers in various domains enabling Continuous Learning.**
- **Developing Entrepreneurial acumen to venture into Innovative areas.**
- **Imparting Value based Professional Education with a sense of Social Responsibility.**

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Vision of the Department

To achieve academic excellence in Electronics and Communication engineering by imparting quality technical education and facilitating research activities

Mission of the department

M1: Establishing state of the art laboratory facilities and infrastructure to develop the spirit of innovation and entrepreneurship

M2: Nurturing the students with technical expertise along with professional ethics to provide solutions for societal needs

M3: Encourage lifelong learning and research among the students and faculty

Program Educational Objectives:

After successful completion of the program,

PEO1: Graduates of the program will have successful technical and professional career in engineering, technology and multidisciplinary environments.

PEO2: Graduates of the program will utilize their knowledge, technical and communication skills to propose optimal solutions to problems related to society in the field of Electronics and Communication.

PEO3: Graduates of the program will exhibit good interpersonal skills, leadership qualities

INSTRUCTIONS:

1) Test the components/devices before starting experiment
2) After rigging up the circuits do not switch on the power supply, show the circuit to lab incharge and then start the experiment.
3) Conduct the experiment as per procedure.
4) Record the readings as per instructions.
5) Confirm successful completion of experiments by plotting the relevant graphs and calculations.
6) After completion of experiment replace the components in their respective positions.
7) Negligence of one candidate will result in penalty for the whole group/batch.
8) Keep components and test Devices in good condition. Replace probes, wires and components at the first sign of deterioration.
9) Don't work on equipment before you know proper procedures.
10) Keep the lab Clean.

CONTENTS

1. Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances

AIM: Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain bandwidth product from its frequency response.

Components Required:

Sl. No	Components	Range	Quantity
1	Resistors	1.5KΩ,6KΏ,2KΩ, 14kΩ,2.3KΩ,10KΩ	each1
2	Capacitors	28pF, 10pF,720pF	3
3	Transistor	BC107	2

Theory:

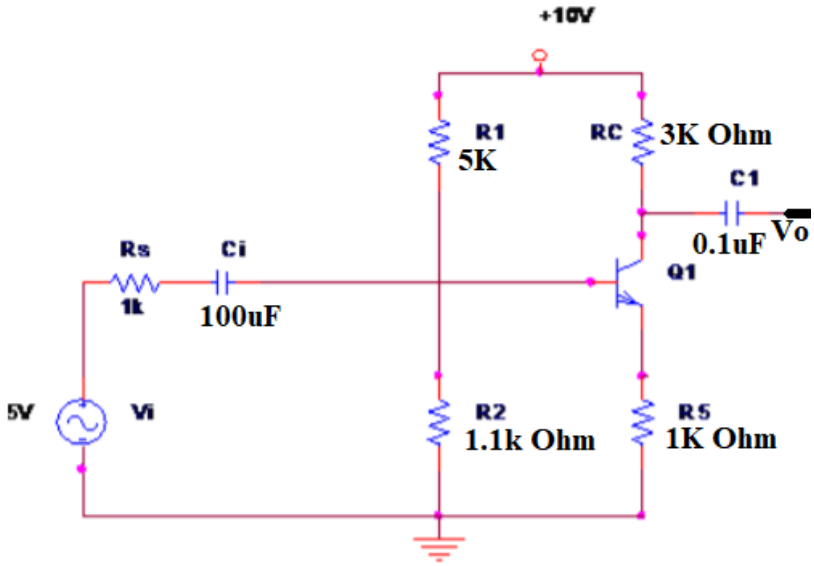
Negative feedback in general increases the bandwidth of the transfer function stabilized by the specific type of feedback used in a circuit. In Voltage shunt feedback amplifier, consider a common emitter stage with a resistance R‟ connected from collector to base. This is a case of voltage shunt feedback and we expect the bandwidth of the Trans resistance to be improved due to the feedback through R‟. The voltage source is represented by its Norton‟s equivalent current source Is=Vs/Rs.

Design:

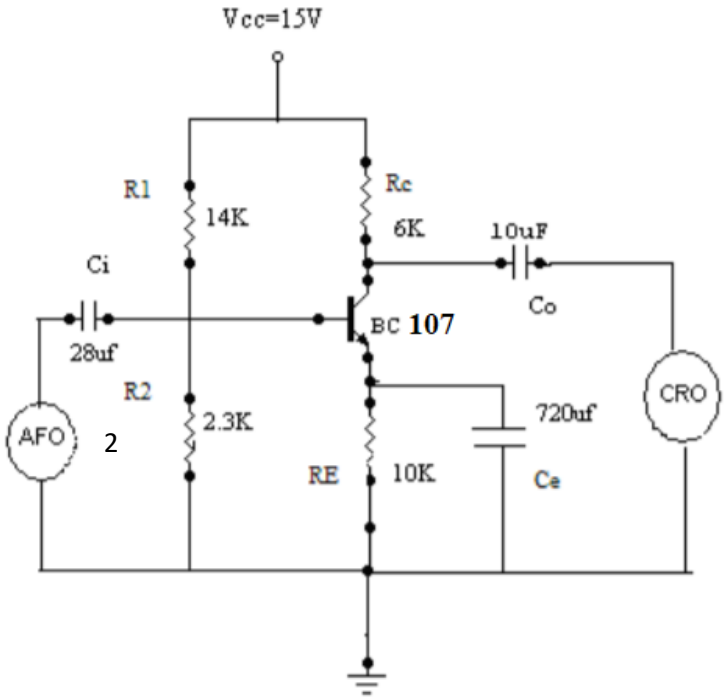
Given specifications:
VCC= 10V, IC=1.2mA, AV= 30, fI = 1 kHz, S=2, hFE= 150, β=0.4
The feedback factor, β= - 1/RF= +1/0.4=2.5KΏ
(i) To calculate RC:
The voltage gain is given by,
AV= -hfe (RC|| RF) / hie
h ie = β re
re = 26mV / IE = 26mV / 1.2mA = 21.6
hie = 150 x 21.6 =3.2K
Apply KVL to output loop,
VCC= IC RC + VCE+ IE RE ----- (1)
Where VE = IE RE (IC= IE)
VE= VCC / 10= 1V
Therefore RE= 1/1.2x10-3=0.8K= 1KΏ
VCE= VCC/2= 5V
From equation (1), RC= 3 KΏ
(ii) To calculate R1&R2:
S=1+ (RB/RE)
RB= (S-1) RE= R1 || R2 =1KΏ
RB= R 1R2 / R1+ R2------- (2)
VB= VBE + VE = 0.7+ 1= 1.7V
VB= VCC R2 / R1+ R2 ------- (3)
Solving equation (2) & (3),
R1= 5 KΏ & R2= 1.1KΏ

CIRCUIT DIAGRAM:

Without Feedback:



With Feedback:



Procedure:

1. Connect the circuit as per the circuit diagram.

2. Set VCC = 10V; set input voltage using audio frequency oscillator.

3. By varying audio frequency oscillator take down output frequency oscillator voltage for difference in frequency.

4. Calculate the gain in dB

5. Plot gain Vs frequency curve in semi-log sheet.

6. Connect the circuit as per the circuit diagram.

7. Set VCC = 10V; set input voltage using audio frequency oscillator.

8. By varying audio frequency oscillator take down output frequency oscillator voltage for difference in frequency.

9. Calculate the gain in dB

10. Plot gain Vs frequency curve in semi-log sheet.

11. Compare this response with respect to the amplifier without feedback.

TABULATION:
(With or without feedback)

FREQUENCY	OUTPUT VO(V)	Vin(V)	Gain = 20log(Vo/Vin) dB

Result:

Determine the gain- bandwidth product, input and output impedances

VIVA QUESTIONS:

1. Explain Operation of Amplification in BJT Common Source CE Amplifier with Feedback
2. Define Feedback and Without feedback Concept in amplifiers.

2A. BJT COLPITT'S OSCILLTOR

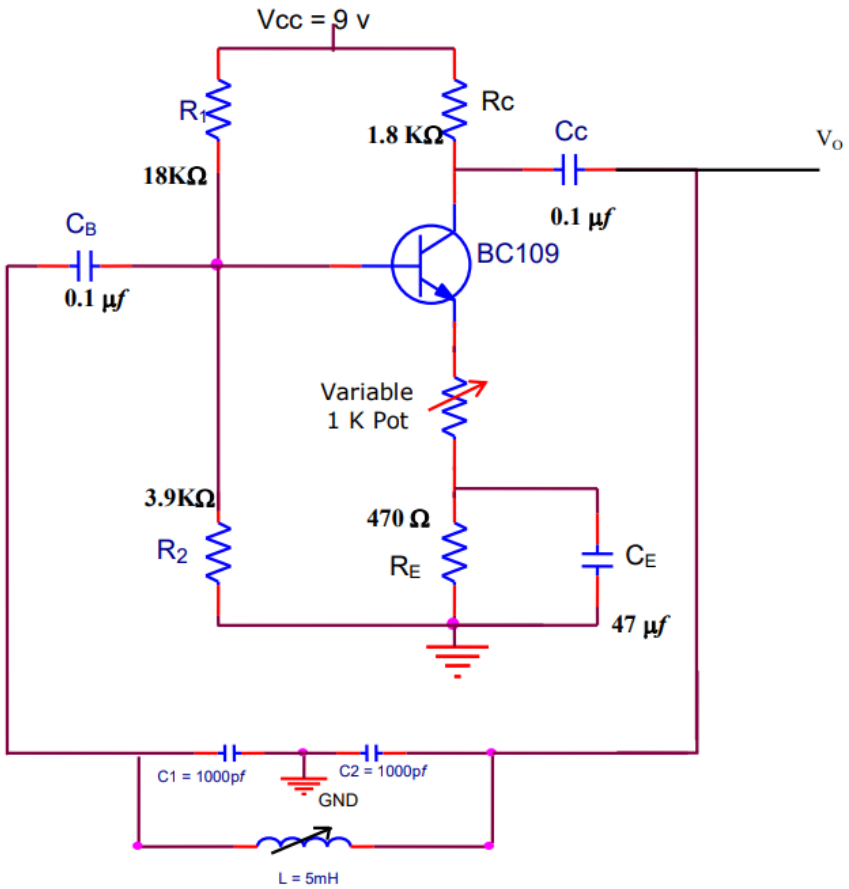
AIM: To design and construct a BJT Colpitt's oscillator at the given operating frequency.

Components Required:

Sl.No	Components	Range	Quantity
1	Transistor	BC107	1
2	Resistors	18K, 1.8KΩ, 3.9K,470Ω	each1
3	Inductor	5mH	1
4	Capacitors	1000pF,0.1 µF	2

Theory: Colpitt's oscillator is very popular and is commonly used as local oscillator in radio receivers. The collector voltage is applied to the collector through inductor L whose reactance is high compared with X2 and may therefore be omitted from equivalent circuit, at zero frequency. The circuit operates as Class C. the tuned circuit determines basically the frequency of oscillation.

CIRCUIT DIAGRAM



Design:

Given V_{CC} = 9V, I_C = 2mA, β = 50

R_E: W.K.T. $V_{RE} = V_{CC} / 10 = 9 / 10 = 0.9V$ ------for biasing

$I_E \approx I_C = 2$ mA

From the fig. We see that, $I_E R_E = V_{RE}$

$R_E = 0.9 / (2 \times 10^{-3}) = 450\Omega$

Therefore **$R_E \approx 470\Omega$**

R_C: $V_{CE} = V_{CC} / 2 = 4.5V$ ----- for Q point to be in active region.

Applying KVL to output loop

$V_{CC} - I_C R_C - V_{CE} - V_{RE} = 0$

$9 - 2 \times 10^{-3} R_C - 4.5 - 0.9 = 0$

Therefore $R_C = 1.8k\Omega$ **R_1 & R_2**: From biasing circuit

$V_B = V_{BE} + V_{RE} = 0.7 + 0.9$ $V_B = 1.6V$

Assume 10 I_B flows through R_1 and 9 I_B flows through R_2.

W.K.T. $I_C = \beta I_B$

$2 \times 10^{-3} = 50\ I_B$

Therefore $I_B = 40\ \mu A$

From the fig. we see that, $R_1 = V_{CC} - V_B / 10$

$I_B = 9 - 1.6 / (10 \times 40 \times 10^{-6}) = 18.5k\Omega$

Therefore $R_1 \approx 18k\Omega$

$R_2 = V_B / 9I_B = 1.6 / (9 \times 40 \times 10^{-6}) = 4.44k\Omega$ Therefore $R_2 \approx 3.9k\Omega$

C_E, C_C, C_B : Let $C_B = C_C = 0.1\mu F$

$X_{CE} = R_E/10$

Therefore $f = 10 / (2\pi\ C_E\ R_E)$

Let f = 100Hz and W.K.T $R_E = 470\Omega$

Therefore $C_E = 10 / 2\pi\ f.R_E = 34\mu F$ Therefore $C_E \approx 47\mu F$.

DESIGN OF TANK CIRCUIT

Assume = f_o = 100 KHz

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

where $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$, Assume $C_1 = C_2 = 1000$ pF

$\therefore$ Ceq = $0.05 * 10^{-6}$ On solving L = 5 mH (Use decade inductance box)

PROCEDURE:

1. Rig up the circuit as shown in the circuit diagram.
2. Before connecting the feedback network, check the circuit for biasing conditions i.e. check V_{CE}, and V_{RE}.
3. After connecting the feedback network. Check the output.
4. Check for the sinusoidal waveform at output. Note down the frequency of the output waveform and check for any deviation from the designed value of the frequency.
5. To get a sinusoidal waveform adjust 1KΩ potentiometer.
6. DCB/DIB can be varied to vary the frequency of the output waveform

RESULT: The Colpitt's oscillator is designed and constructed for the given frequency.

2 B. BJT-CRYSTAL OSCILLATOR

AIM: Testing for the performance of the BJT- crystal oscillator for f_o> 500KHz.

Components Required:

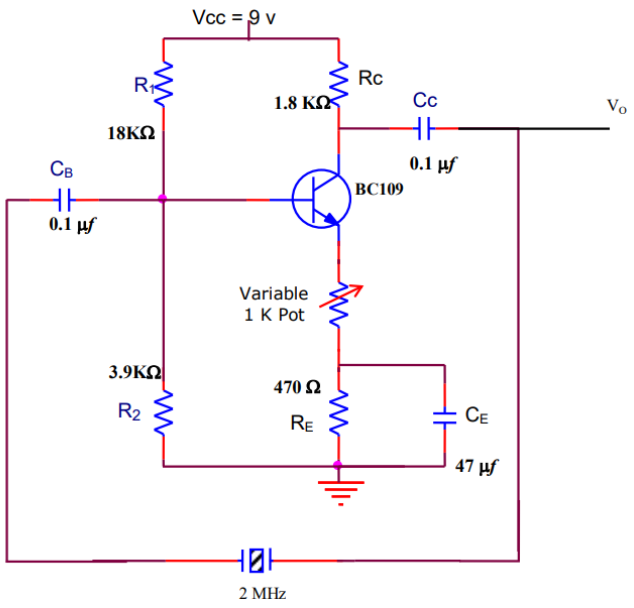
Sl.No	Components	Range	Quantity
1	Transistor	BC107	1
	Resistors	18K, 1.8KΩ, 3.9K,470Ω	each1
	Resistors	1KΩ	2
2	Capacitors	47µF,0.1 µF	2

Theory: A crystal oscillator is basically a tuned oscillator using a piezoelectric crystal as a resonant circuit. The crystal has a greatest stability in holding consent charge at whatever frequency the crystal is originally cut to operate. Crystal oscillators are used whenever great stability is required, such as communication, transmitters and receivers.

Characteristics of a Quartz crystal: A quartz crystal exhibits the property that whenever mechanical stress is applied across one set of its faces, a difference of potential develops across the opposite faces. This property of a crystal is called piezoelectric effect. Similarly, a voltage applied across one set of faces of the crystal causes mechanical distortion in the crystal shape. When alternating voltage is applied to a crystal, mechanical vibrations are set up- these vibrations having a natural resonating frequency dependent on the crystal.

The inductor L and the capacitor C represent electrical equivalents of crystal mass and compliance respectively, whereas resistance R is an electrical equivalent of the crystal structures internal friction. The shunt capacitance CM represents the capacitance due to mechanical mounting of the crystal. Because the crystal loses, represented by R, are small, the equivalent crystal Q factor is high typically 20,000. Values of Q up to almost 106 can be achieved by using crystals. The crystal has two resonant frequencies. One resonant condition occurs when the reactances of the series RLC leg are equal.

CIRCUIT DIAGRAM:



Design:

Given V_{CC} = 9V, I_C = 2mA, β = 50

RE: W.K.T. $V_{RE} = V_{CC} / 10 = 9 / 10 = 0.9V$ ------for biasing
$I_E \approx I_C = 2$ mA
From the fig. We see that, $I_E R_E = V_{RE}$ $R_E = 0.9 / (2 \times 10^{-3}) = 450\Omega$
Therefore **RE ≈ 470Ω**

RC: $V_{CE} = V_{CC} / 2 = 4.5V$ ----- for Q point to be in active region.
Applying KVL to output loop $V_{CC} - I_C R_C - V_{CE} - V_{RE} = 0$
$9 - 2 \times 10^{-3} R_C - 4.5 - 0.9 = 0$
Therefore **RC = 1.8kΩ**

R_1 & R_2: From biasing circuit $V_B = V_{BE} + V_{RE} = 0.7 + 0.9$ $V_B = 1.6V$
Assume 10 I_B flows through $R_1$and 9 I_B flows through R_2.
W.K.T. $I_C = \beta I_B$ $2 \times 10^{-3} = 50$ I_B Therefore $I_B = 40$ μA
From the fig. we see that, $R_1 = V_{CC} - V_B / 10$ $I_B = 9 - 1.6 / (10 \times 40 \times 10^{-6}) =$ **18.5kΩ**
Therefore $R_1 \approx 18k\Omega$ R2 = $V_B / 9I_B = 1.6 / (9 \times 40 \times 10^{-6}) =$ **4.44kΩ**
Therefore **$R_2 \approx 3.9k\Omega$**
C_E, C_C, C_B : Let $C_B = C_C = 0.1\mu F$ $X_{CE} = R_E/10$ Therefore $f = 10 / (2\pi C_E R_E)$
Let and **f = 100Hz** W.K.T $R_E = 470\Omega$ Therefore $C_E = 10 / 2\pi f.R_E = 34\mu F$ Therefore **$C_E \approx 47\mu F$.**

PROCEDURE:

1. Rig up the circuit as shown in the circuit diagram.
2. Before connecting the feedback network, check the circuit for biasing conditions i.e. check VCE, and VRE.
3. After connecting the feedback network. Check the output.
4. Check for the sinusoidal waveform at output. Note down the frequency of the output waveform and check for any deviation from the designed value of the frequency.
5. To get a sinusoidal waveform adjust 1KΩ potentiometer

RESULT: The crystal oscillator is designed and constructed for the given frequency

3 A. Design Adder, Integrator and Differentiator circuits using Op-Amp.

AIM: Design Adder using Op-Amp

Components required:

Sl.No.	Particulars	Specification	Quantity
1.	OP AMP	uA741	01
2.	Resistors	1Kohm	04

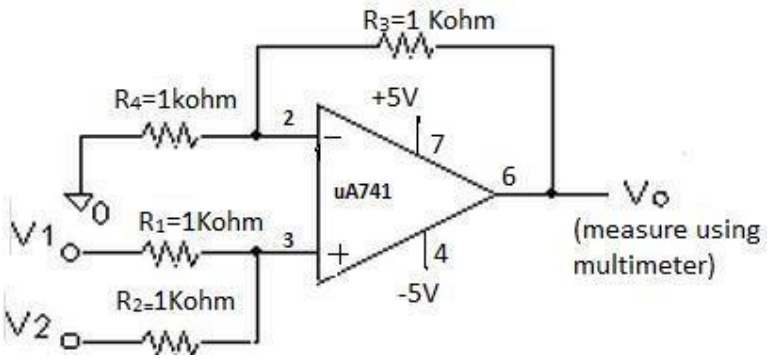
Theory:

Adder is one of the liner applications of the Op-Amp. A circuit whose output is the sum of several input signals is called a Summer (Adder). The output is

Procedure:

1. Connections are made as shown in the circuit diagram.
2. Apply DC input V1 and V2 of various values and tabulate the output of Op-AmpV0

Circuit Diagram



Design: Adder is one of the liner applications of the Op-Amp. A circuit whose output is the sum of several input signals is called a Summer (Adder). The output is $V_0 = \left(\frac{R_3+R_4}{R_4}\right)\left(\frac{v_1+v_2}{2}\right)$

Tabular Column:

V1	V2	Theoretical o/p (Vth)	Practical o/p(V0= V1+V2)
0.5	0.5		
1	1		
1	0.5		
0.5	2		

B. INTEGRATOR AND DIFFERENTIATOR USING OP-AMP

AIM: To design and test the performance of integrator and differentiator circuits using Op-amp.

COMPONENTS REQUIRED:

Sl. No.	Particulars		Specification	Quantity
1.	OP AMP		uA741	01
2.	Resistors		1Kohm	04
3.	Capacitor		0.01uF	02

THEORY:

Integrator: In an integrator circuit, the output voltage is integral of the input signal. The output voltage of an integrator is given by $V_o = -1/R_1C_f \int_t Vidt$

At low frequencies the gain becomes infinite, so the capacitor is fully charged and behaves like an open circuit. The gain of an integrator at low frequency can be limited by connecting a resistor in shunt with capacitor.

Differentiator: In the differentiator circuit the output voltage is the differentiation of the input voltage.

The output voltage of a differentiator is given by $V_o = -RfC_1\frac{dV_i}{dt}$ The input impedance of this circuit decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise. At high frequencies circuit may become unstable

DESIGN:

INTEGRATOR:

Given :

$R1 = 10\ K\Omega$; $f = 4$ kHz

$C_f = 1/ (2\pi Rf)$

$R_f = 10\ R = 10 * 10\ K\Omega = 100\ K\Omega$

$C_f = 1/ (2\pi * 10^3 * 10 * 4 * 10^3) = 0.039\ \mu f$

DIFFERENTIATOR:

Given:

$C_1 = 1\ \mu f$; $f_1 = 150$ kHz $R_f = 1/ (2\pi C_1 f_1) =$

$= 1/ (2*3.14*1*10^{-6}*150)$

$R_f = 1.06\ K\Omega$

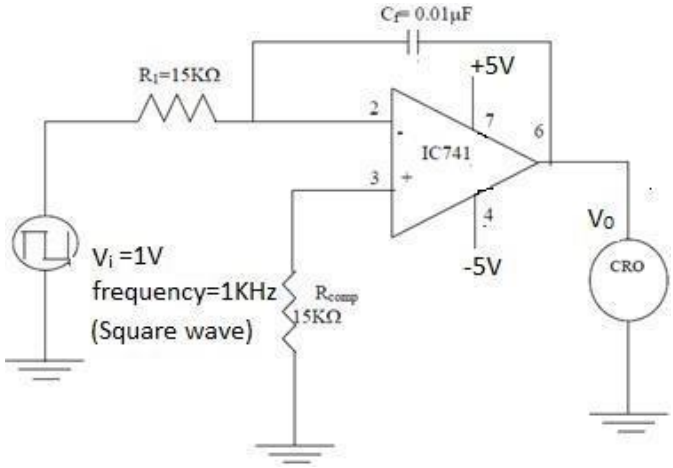
$C_f = R_1C_1/R_f$

$$= \frac{1.06*10^{-3}*0.1*10^{-6}}{10.6 * 10^{3}}$$

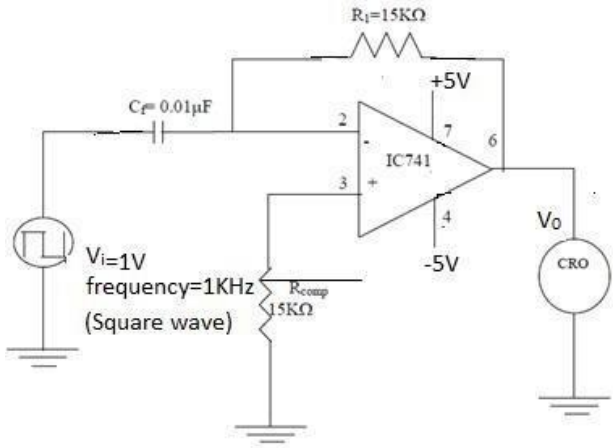
$C_f = 0.01\mu f$ and $R_f = 100K\Omega$

Circuit Diagram

1) Integrator



2) Differentiator



Input and output Waveforms:

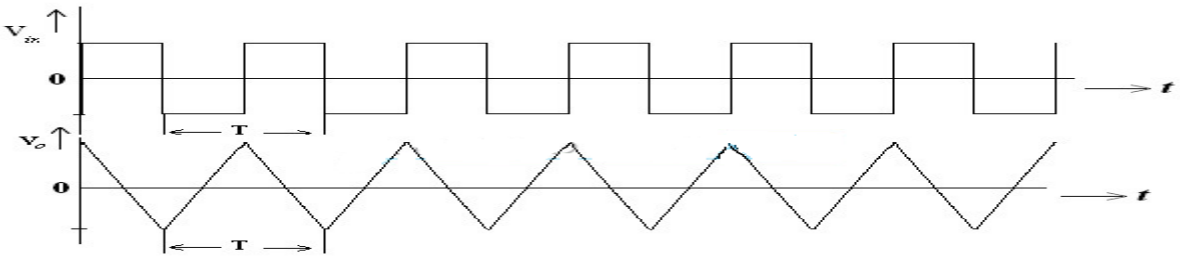


Fig: Input and Output Waveforms of an Integrator

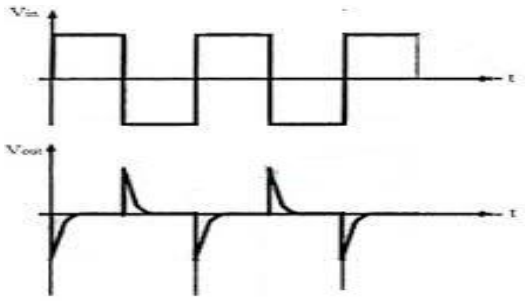


Fig: Input and Output waveforms for Differentiator

PROCEDURE:

Integrator:
1. Connections are made as per the circuitdiagram.
2. Apply the square or sine input signal at high frequency usingAFO.
3. Note the corresponding output waveforms and plot thegraph.

Differentiator:
1. Connections are made as per the circuitdiagram.
2. Apply the square or sine input signal at low frequency usingAFO.
3. Note the corresponding output waveforms and plot thegraph.

Result:
Output waveforms are observed on CRO

Viva questions :

1. What are the limitations of the basic differentiator circuit:
2. Mention the Applications of Integrator/Differentiator
3. How Opamp works as Integrator/Differentiator

4A STATIC CHARACTERISTICS OF SCR

AIM: To obtain the static characteristics of SCR and to determine latching current and holding current.

Components Required: Resistors : 1kΩ / 1/2W, 5 kΩ /5W.

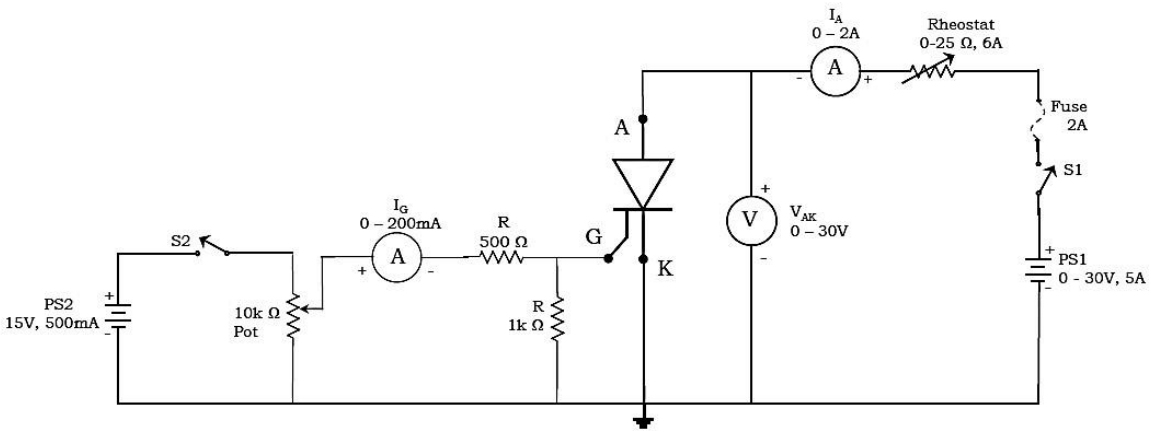
Ammeters : 0 – 100mA, 0 – 50mA.

Voltmeter : 0 – 300V.

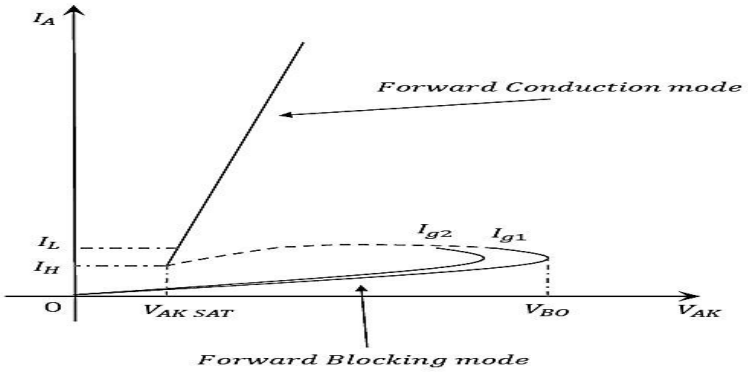
SCR : TYN616

Power supply: 0 – 300V, 0 – 30V

CIRCUIT DIAGRAM



WAVEFORMS



Tabular Column:

V_{BO} = ------- volts, I_{G1}= -----mA

V_{AK} (V)	I_{AK} (mA)

Latching current I_L = ----- Holding

current I_H = -----

$I_L = 3\ I_H$

Procedure:

a)Determination of latching current:

1) Rig up the circuit as shown in figure.
2) Set supply voltage of power circuit to 100V (V_{BO}).
3) Increase gate supply voltage, until the SCR is triggered then stop.
4) Switch off gate supply voltage and observe whether the SCR is conducting or not. If it is conducting note I_{AK} as latching current I_L.
5) If SCR is switched off when gate is off.
6) Switch ON gate supply voltage and increase I_{AK} and repeat step (4), until SCR is latched.
7) Increase V_S and note corresponding I_{AK} and tabulate the readings.

b)Determination of holding current :

1) Slowly reduce V_S, consequently I_{AK} also reduces in the same speed, but at some level, I_{AK} reduces drastically, the corresponding current is called holding current.
2) Plot VI characteristics and determine ON state resistance R_{ON} from the graph.

Note: For another set of readings (I_{G2}) switch off V_S and V_g and then repeat the Experiment

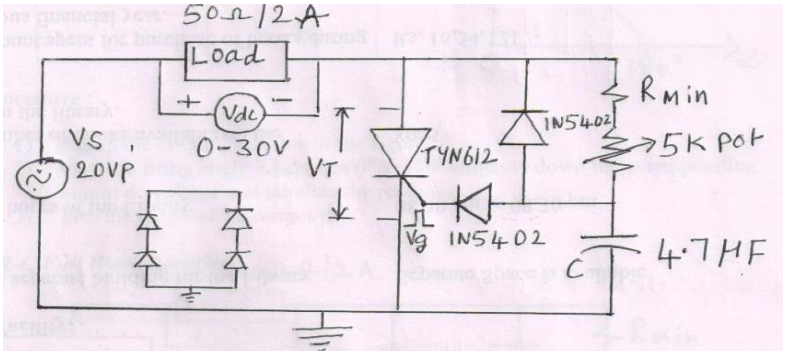
Result: Static characteristics of SCR, latching current and holding current is verified.

4B SCR CONTROLLED HWR AND FWR USING RC

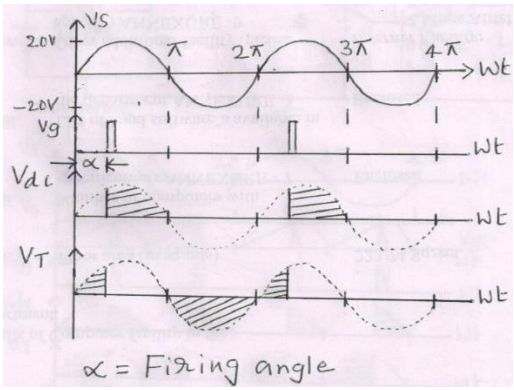
AIM : To study the R-C triggering of SCR in Half Wave and Full Wave modes and hence to plot average o/p voltage V_{dc} v/s firing angle α.

Circuit Diagram:

R-CHalf wave rectifier:



Wave Form:



Tabular Column: $V_{dc}=V_m/2\Pi[1+\cos\alpha]$

Firing angle (α)	V_{dc}(V)

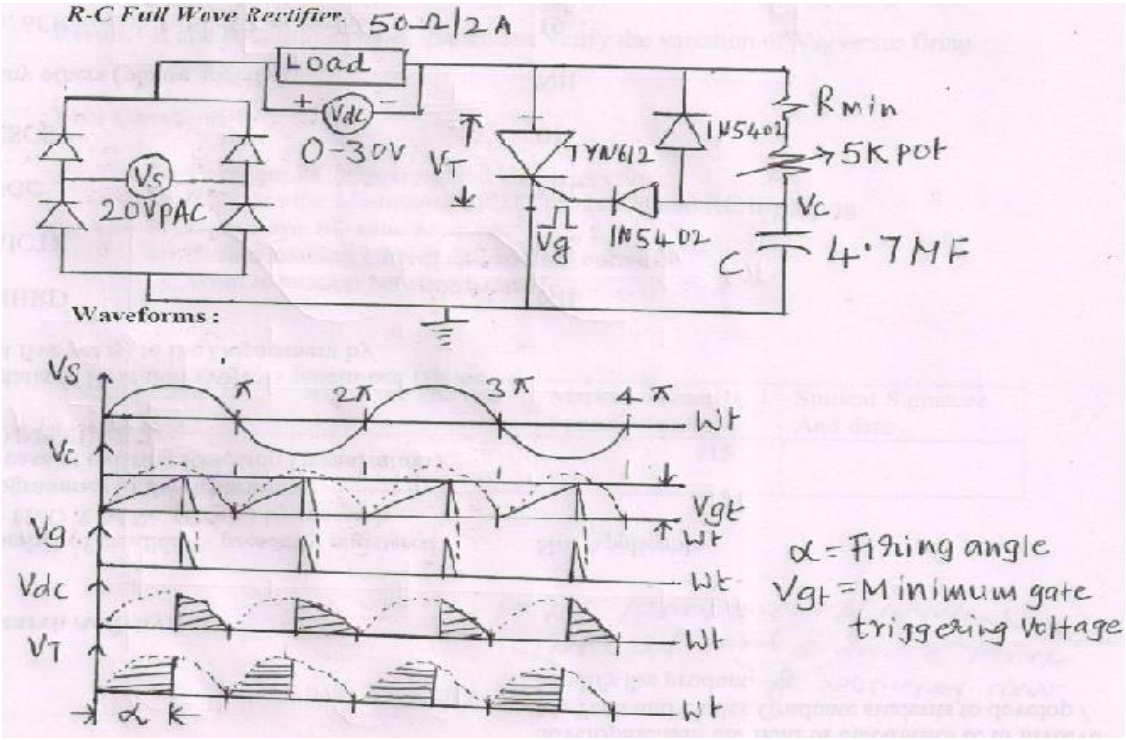
Procedure:

1) Rig up the circuit as shown in the figure.

2) Vary the firing angle α between 0º to 180º and note down the corresponding output dc voltage and tabulate the readings.

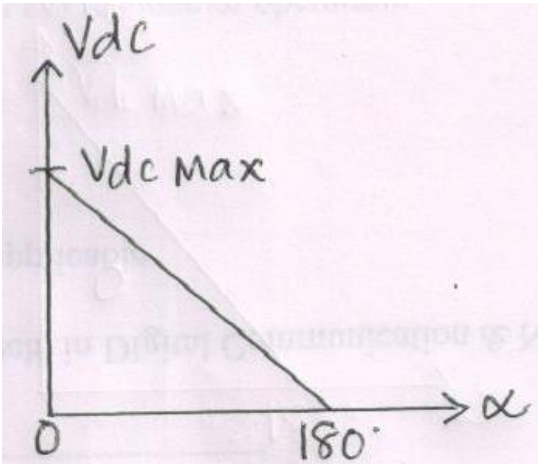
3) Plot the graph of V_{dc} versus α.

RC FULL WAVE RECTIFIER



Tabular Column: $V_{dc} = V_m / \Pi(1 + \cos\alpha)$

Firing Angle (α)	V_{dc} (V)



Procedure :

1) Rig up the circuit as shown in the figure.
2) Vary the firing angle α between 0º to 180º and note down the corresponding output dc voltage and tabulate the readings.
3) plot the graph of V_{dc} versus α

Result:- R and R-C triggering is studied and verify the variation of V

5.Design and implement

(A) Half adder & Full Adder using (i) Basic Gates and (ii) NAND Gates.
(B) Half subtractor & Full subtractor using (i) Basic Gates and (ii) NAND Gates.
(C)**4** -VARIABLE FUNCTION USING IC 74151(8:1MUX).

COMPONENTS REQUIRED:-

Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	AND gate	7408
2	OR gate	7432
3	Not gate	7404
4	EXOR gate	7486
5	Patch chords	
6	Trainer Kit	

(a) HALF-ADDER:

THEORY:

A combinational logic circuit that performs the addition of two data bits, A and B, is called a half-adder. Addition will result in two output bits; one of which is the sum bit, S, and the other is the carry bit, C. The Boolean functions describing the half-adder are:

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

For Carry

A \ B	0	1
0	0	0
1	0	1

Carry = AB

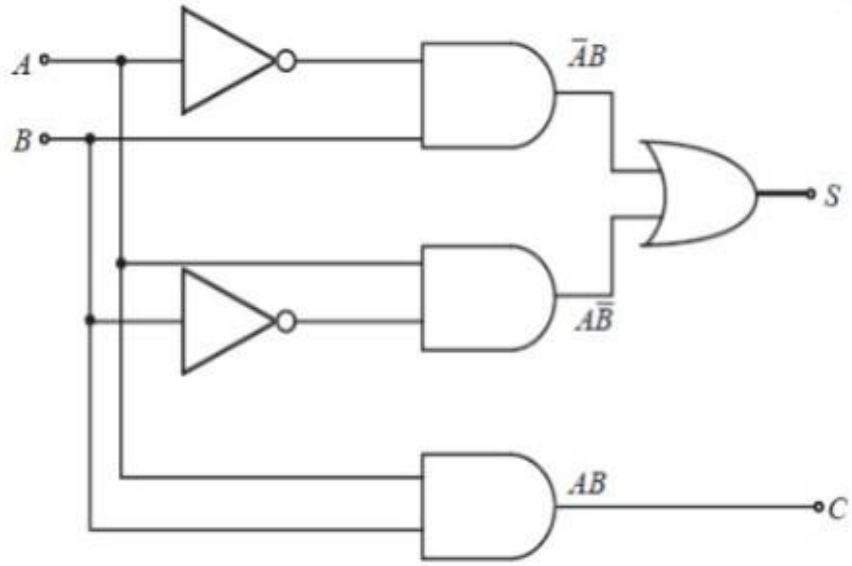
For Sum

A \ B	0	1
0	0	1
1	1	0

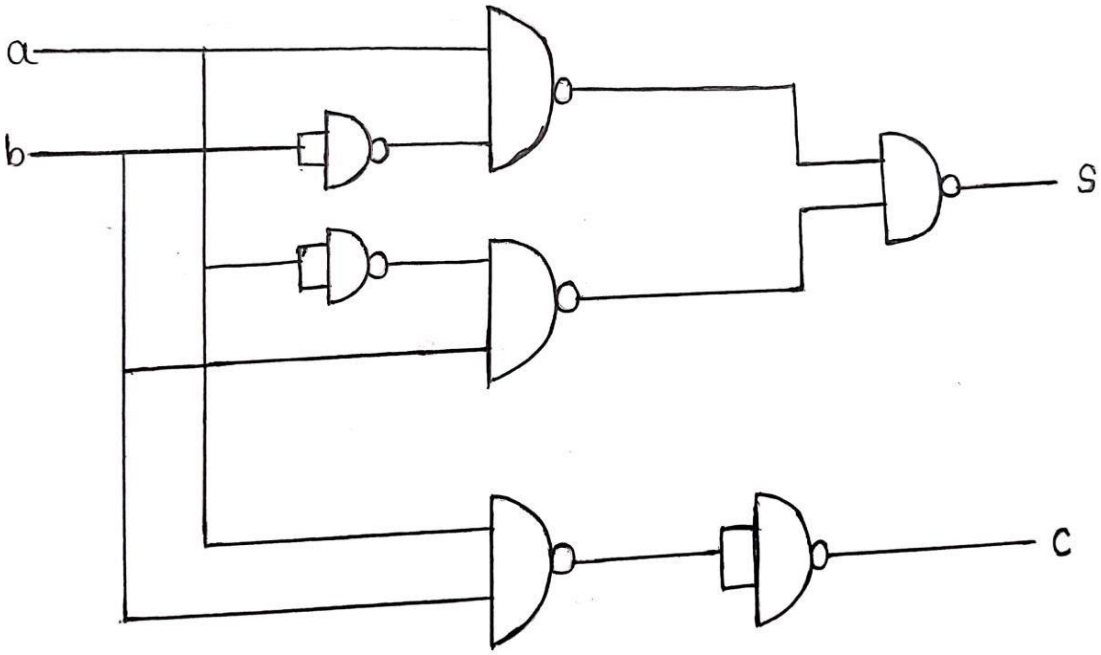
Sum = $A\bar{B} + \bar{A}B$
= $A \oplus B$

Logic Diagram :

(i) Basic Gates:



(ii) NAND Gates:

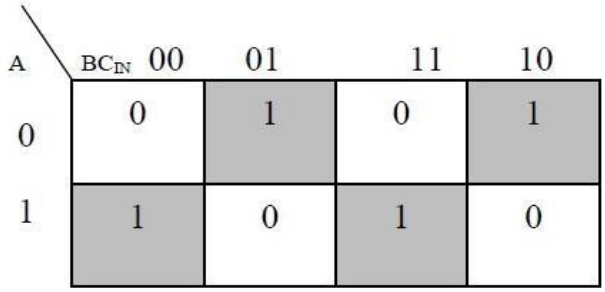


FULL-ADDER: The half-adder does not take the carry bit from its previous stage into account. This carry bit from its previous stage is called carry-in bit. A combinational logic circuit that adds two data bits, A and B, and a carry-in bit, Cin, is called a full-adder. The Boolean functions describing the full-adder are:

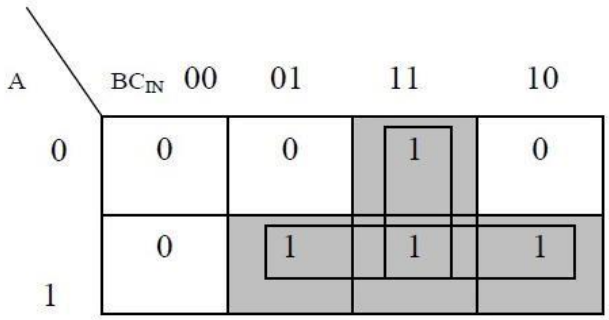
Truth Table:

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K – MAP Simplification:



$S = \bar{A}\bar{B}\bar{C}in + \bar{A}B\bar{C}\bar{i}n + ABCin$



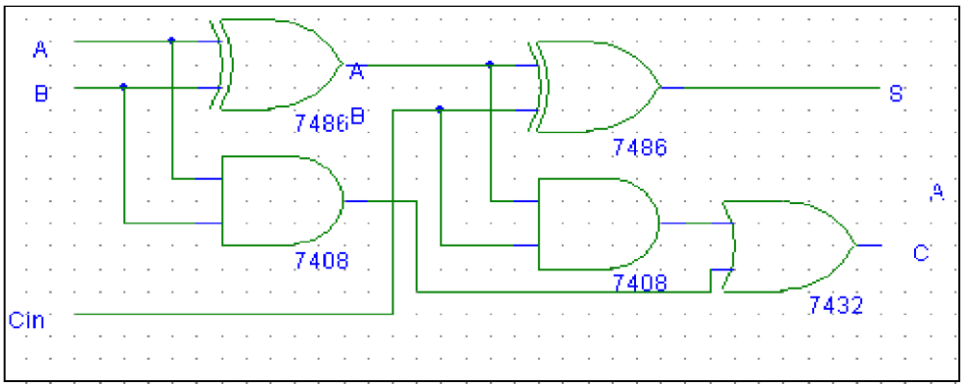
COUT = AB + ACIN + BCIN

Boolean Expression:

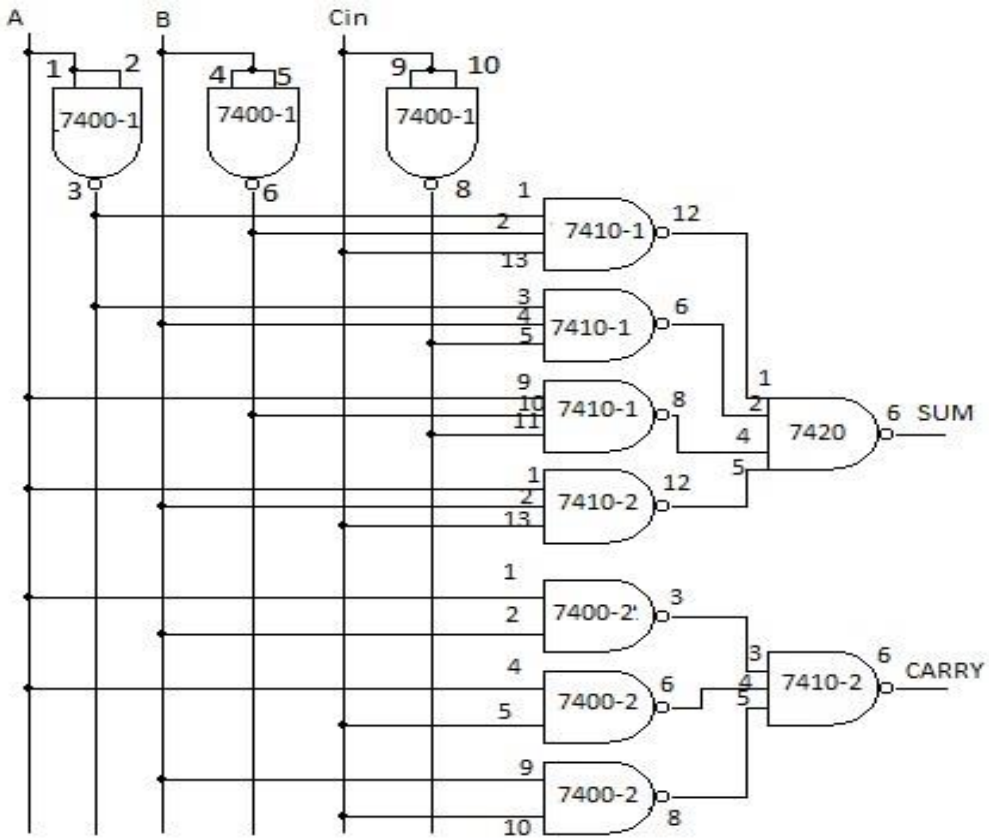
$$S = A \oplus B \oplus Cin$$
$$C = A.B + Cin\ (A \oplus B)$$

Logic Diagram:

(a) BASIC GATES



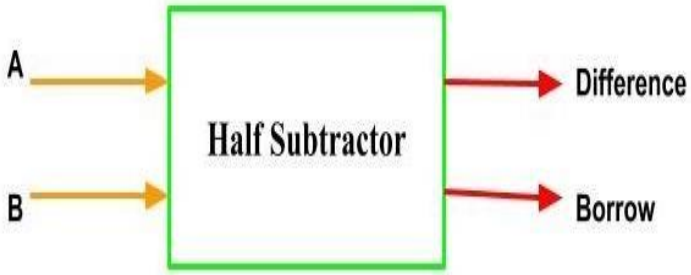
(b)NAND GATES



PROCEDURE:

1. Make connections as shown in the circuit diagram.
2. Connect Vcc and GND to respective pins of IC
3. Switch on the trainer kit
4. Apply inputs using toggle switches and verify the truth table using LEDs.

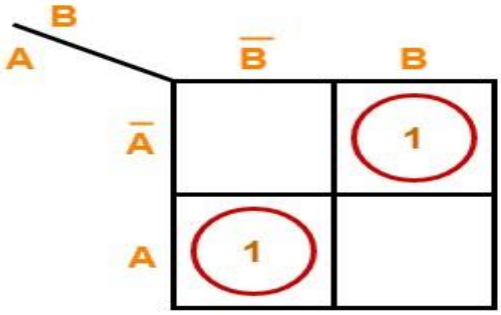
4B. HALF SUBTRACTOR*:* Subtracting a single-bit binary value B from another A (i.e. A B) produces a difference bit D and a borrow out bit B-out. This operation is called half subtraction and the circuit to realize it is called a half subtractor. The Boolean functions describing the half- Subtractor are:



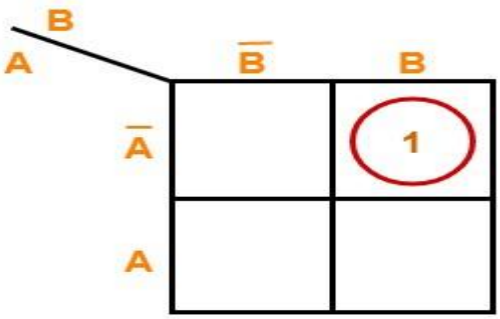
Truth Table:

Input		Output	
A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

K – MAP Simplification:



$D = A \oplus B$



$Brb = \overline{A}.B$

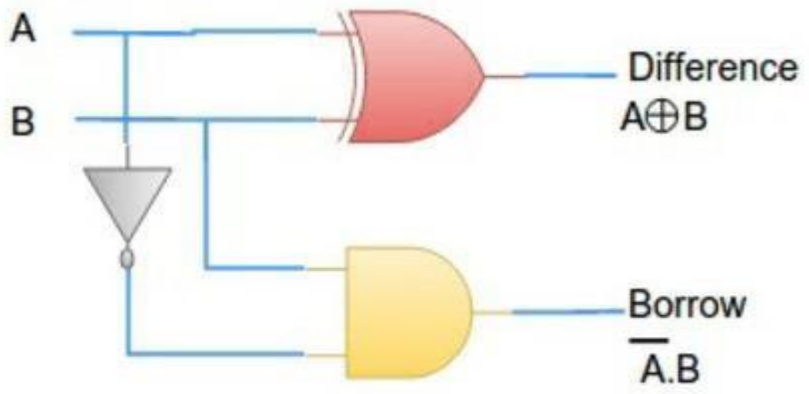
Boolean Expression:

$$D = \overline{A}B + A\overline{B} = A \oplus B$$

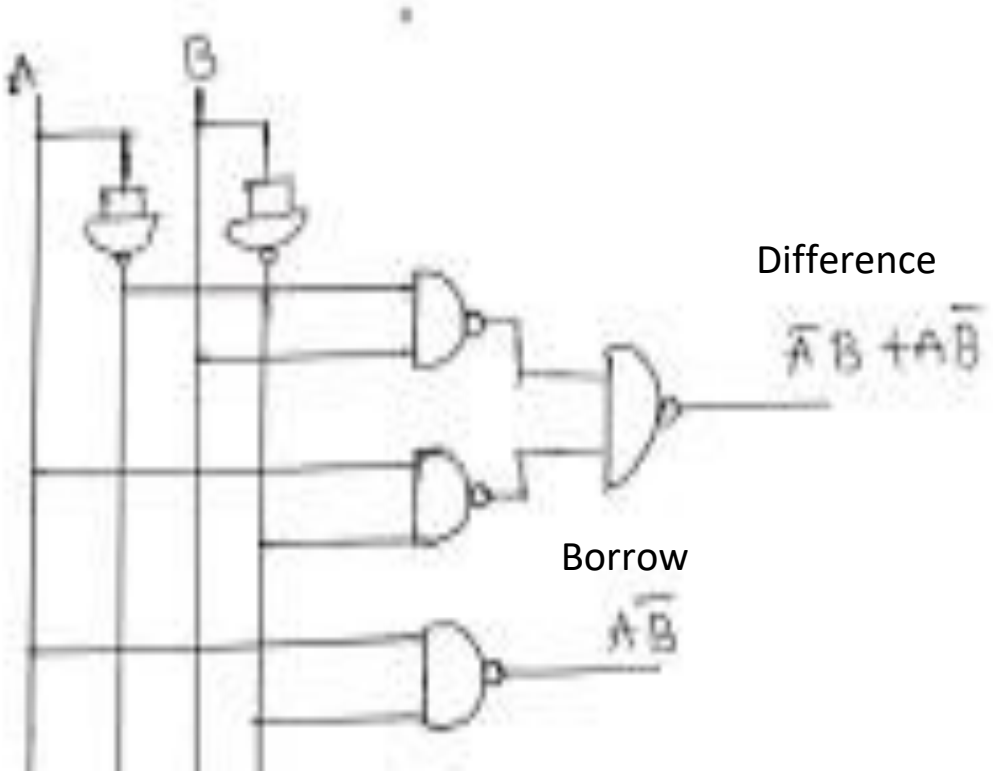
$$Br = \overline{A} \cdot B \text{ Logic}$$

Diagram:

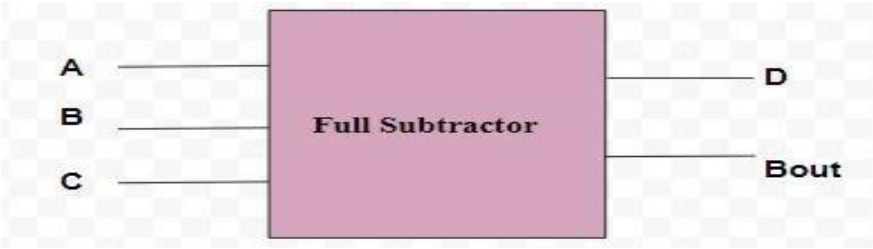
(c) BASIC GATES



(d)NAND GATES



FULL SUBTRACTOR: Subtracting two single-bit binary values, B, Cin from a singlebit value A produces a difference bit D and a borrow out Br bit. This is called full subtraction. The Boolean functions describing the full subtractor are:



(i)TRUTH TABLE:

INPUTS			OUTPUTS	
A	B	Cin	D	Br
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

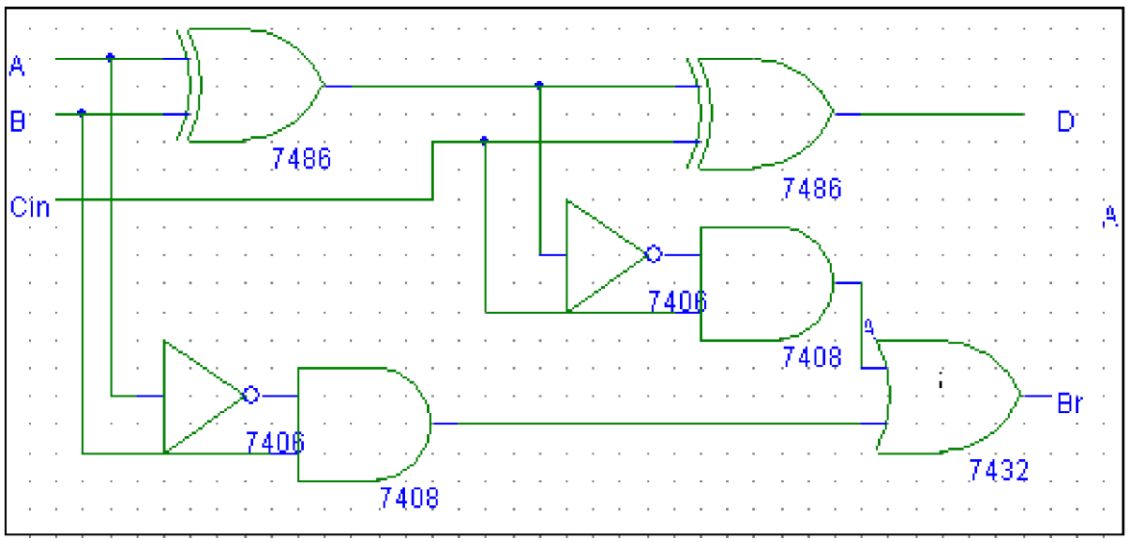
(ii) BOOLEAN EXPRESSION:

$$D = A \oplus B \oplus C$$

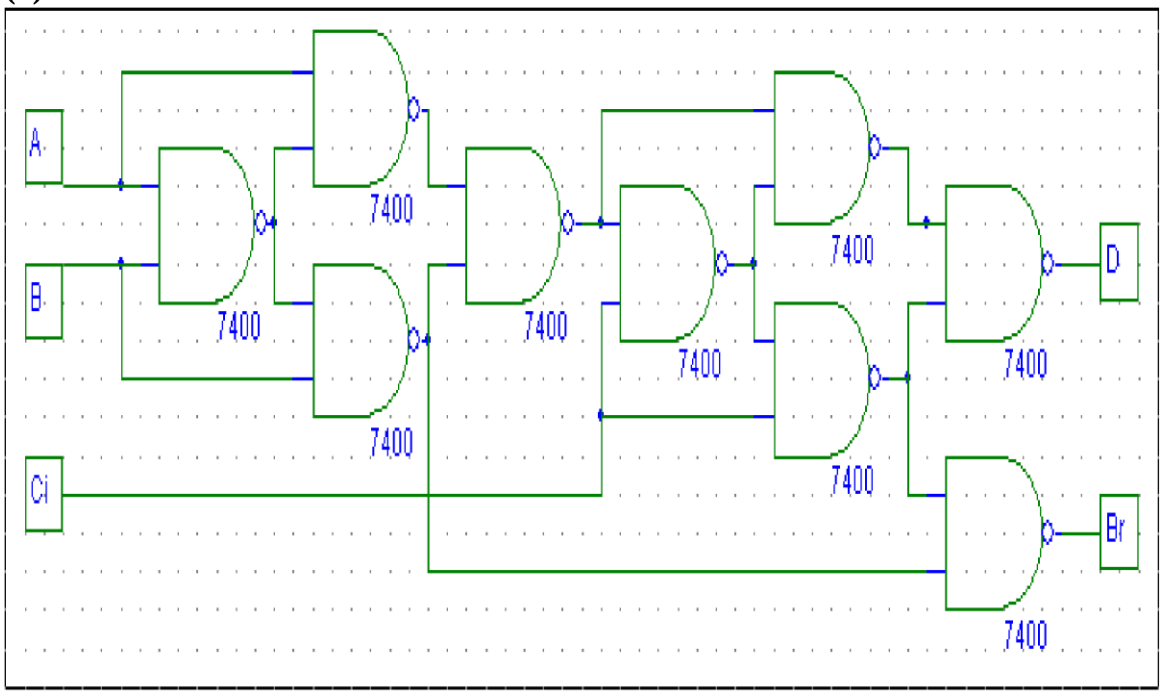
$$Br = \bar{A}\,B + B\,Cin + \bar{A}\,Cin$$

1. LOGIC DIAGRAM:

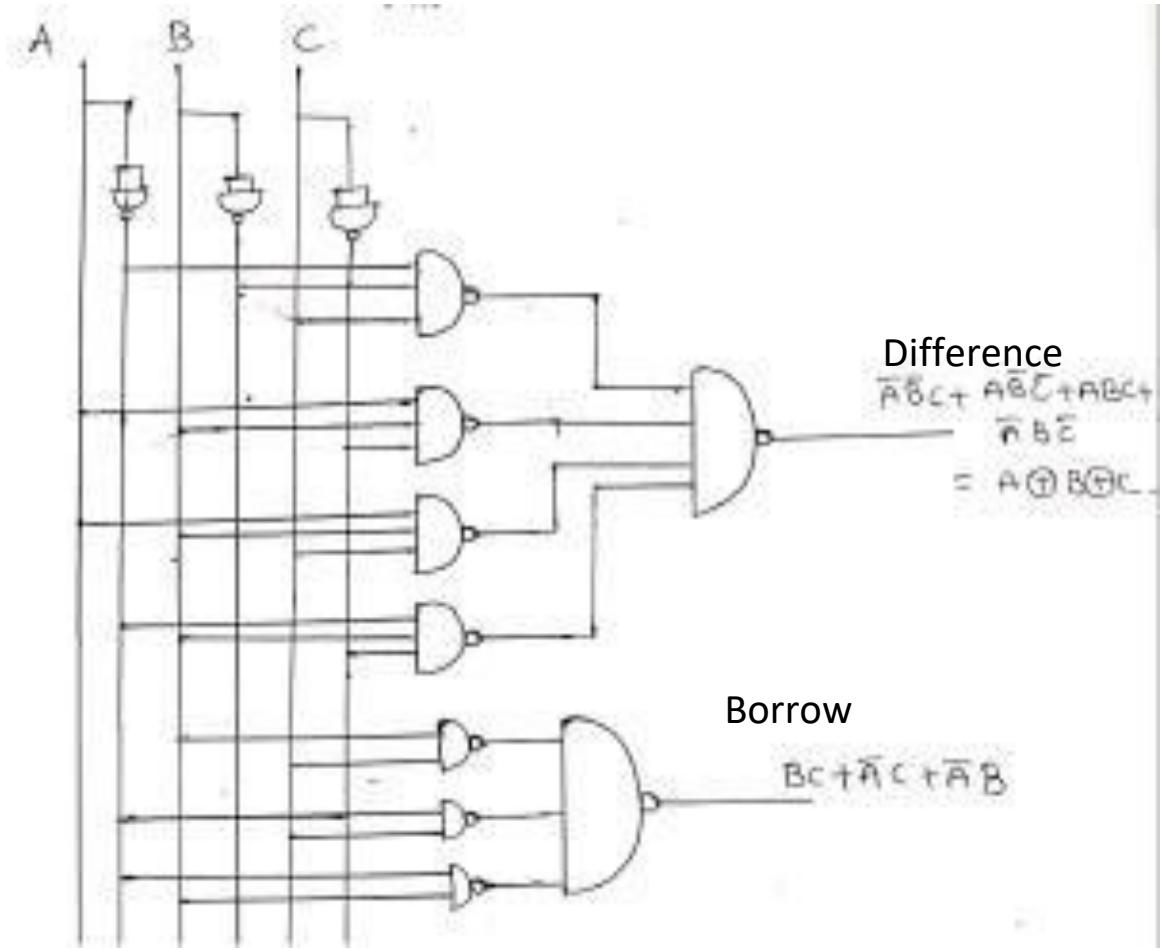
(a)BASIC GATES



(b)NANDGATE



OR



PROCEDURE:

1. Make connections as shown in the circuit diagram.
2. Connect Vcc and GND to respective pins of IC
3. Switch on the trainer kit
4. Apply inputs using toggle switches and verify the truth table using LEDs.

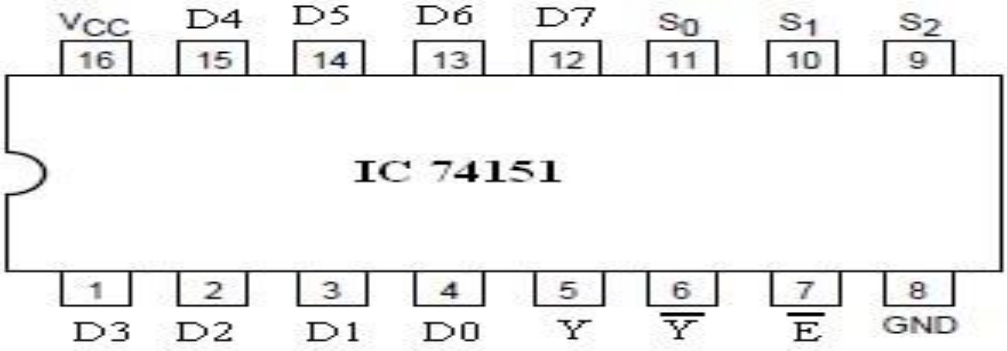
RESULT: Full adder, Full Subtractor circuits are realized using logic gates and the truth tables are verified.

VIVA QUESTIONS:

1. What is a half adder?
2. What is a full adder?
3. What are the applications of adders?
4. What is a half subtractor?
5. What is a full subtractor?
6. What are the applications of subtractors?
7. Obtain the minimal expression for above circuits.
8. Realize a full adder using two half adders
9. Realize a full subtractors using two half subtractors

C. 4 -VARIABLE FUNCTION USING IC 74151(8:1MUX).

- **PIN DETAILS OF 74151:**



EX: Implement the following 4 variable Boolean function using 74151 (8:1 multiplexer). F (A, B, C, D) = ∑m (2, 4, 5, 7, 10, 14)

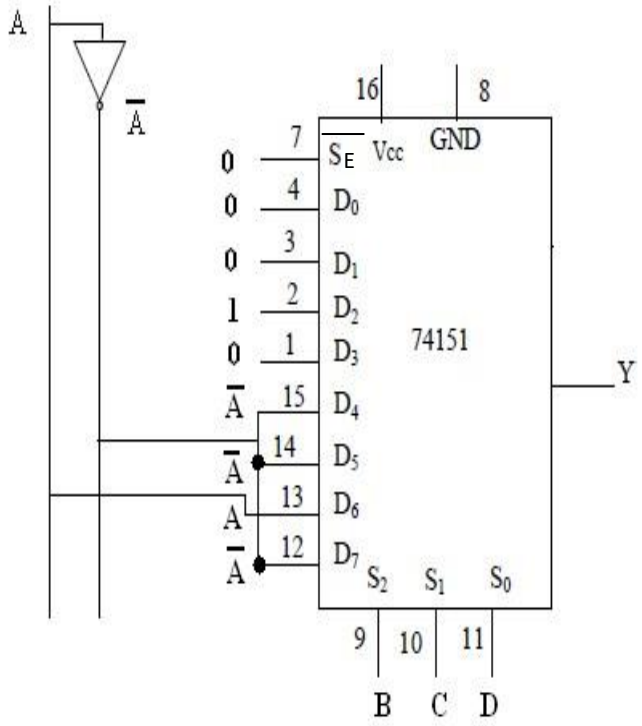
TRUTH TABLE OF 16:1 MUX:

$\overline{\text{Enable}}$	A	B	C	D	Y
1	X	X	X	X	0
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	1
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	1
0	1	1	1	1	0

DESIGN TABLE (Using MSB Bit A)

BCD	D0	D1	D2	D3	D4	D5	D6	D7	
$\overline{A}$	0	1	(2)	3	(4)	(5)	6	(7)	Row 1
A	8	9	(10)	11	12	13	(14)	15	Row 2
I/P To MUX	0	0	1	0	$\overline{A}$	$\overline{A}$	A	$\overline{A}$	

- **LOGIC DIAGRAM:**



RESULT: TheOperation of Multiplexer has been realized and verified with the truth table

6.Realize

A.BINARY TO GRAY CODE CONVERSION USING IC74139
B.BCD to Excess-3 code conversion and vice-versa.

A.Binary to Gray code conversion & vice-versa (74139)

COMPONENTS REQUIRED:-

Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	NAND gate(2 pin)	7400
2	NAND gate(4 pin)	
3	DEMUX	74139
4	Not gate	7404
5	Patch chords	
6	Trainer Kit	

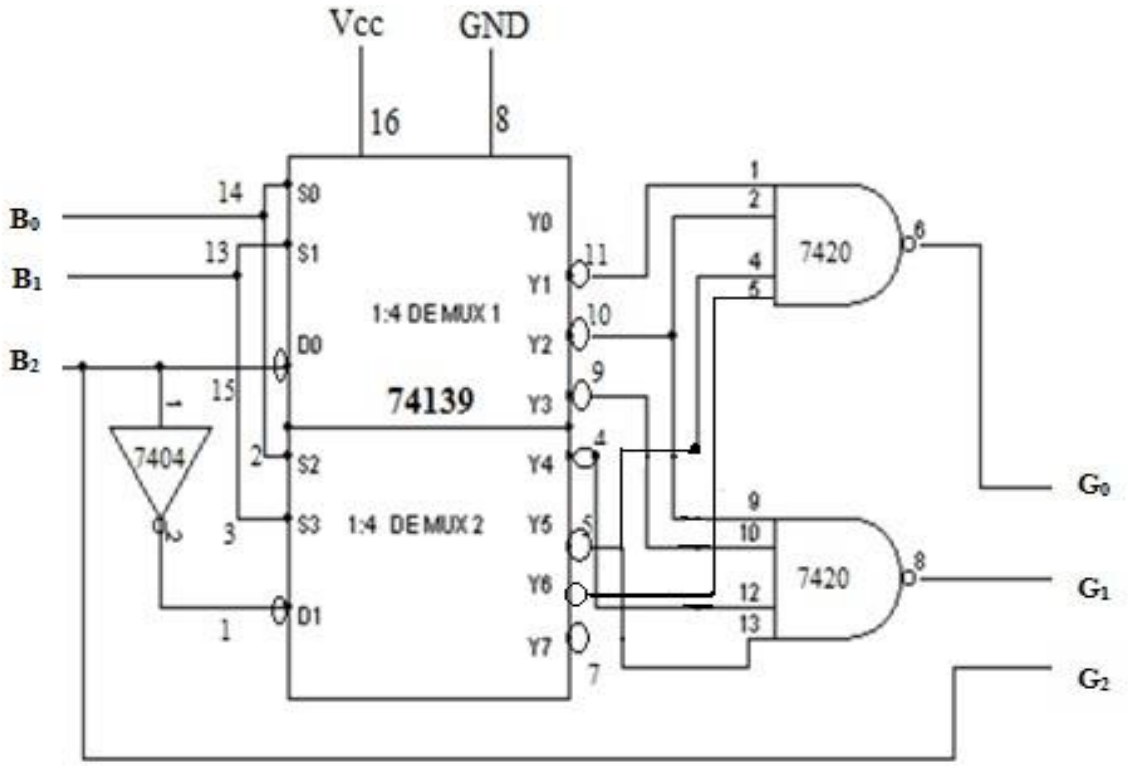
TRUTH TABLE:

BINARY CODE			**GRAY CODE**		
B2	**B1**	**B0**	**G2**	**G1**	**G0**
0	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**0**	**1**
0	**1**	**0**	**0**	**1**	**1**
0	**1**	**1**	**0**	**1**	**0**
1	**0**	**0**	**1**	**1**	**0**
1	**0**	**1**	**1**	**1**	**1**
1	**1**	**0**	**1**	**0**	**1**
1	**1**	**1**	**1**	**0**	**0**

LOGIC DIAGRAM FOR THE FOLLOWING FUNCTION USING IC 74139:

- G0 $=\sum m\ (1,2,5,6)$
- G1 $=\sum m\ (2,3,4,5)$
- G2 $=\sum m\ (4,5,6,7)$

GRAY TO BINARY CODE CONVERSION USING IC74139

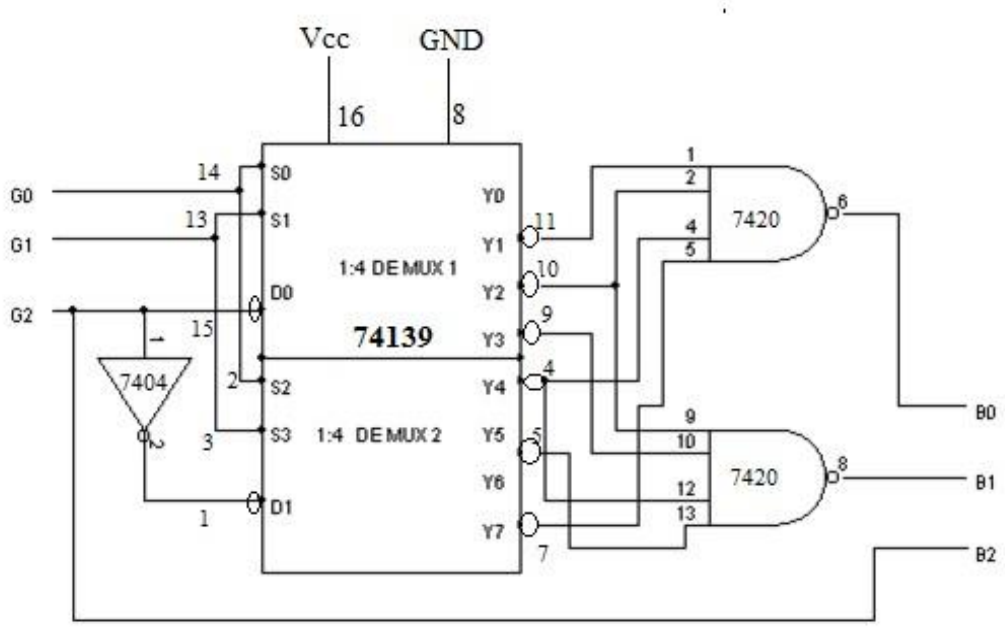


TRUTH TABLE:

GRAY CODE			BINARY CODE		
G2	**G1**	**G0**	**B2**	**B1**	**B0**
0	**0**	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**0**	**1**
0	**1**	**1**	**0**	**1**	**0**
0	**1**	**0**	**0**	**1**	**1**
1	**1**	**0**	**1**	**0**	**0**
1	**1**	**1**	**1**	**0**	**1**
1	**0**	**1**	**1**	**1**	**0**
1	**0**	**0**	**1**	**1**	**1**

LOGIC DIAGRAM FOR THE FOLLOWING FUNCTION USING IC 74139:

- B0 $=\sum m\ (1,2,4,7)$
- B1 $=\sum m\ (2,3,4,5)$
- B2 $=\sum m\ (4,5,6,7)$



Procedure:

1) Rig up the circuit using NAND gates and then with IC74139/38 as shown in figure.
2) Verify the output with the truth table Value
3) The output obtained practically should match the required result.

Result: Operation of Decoder and their applications in Code Converters has been realized and verified.

Viva Questions:

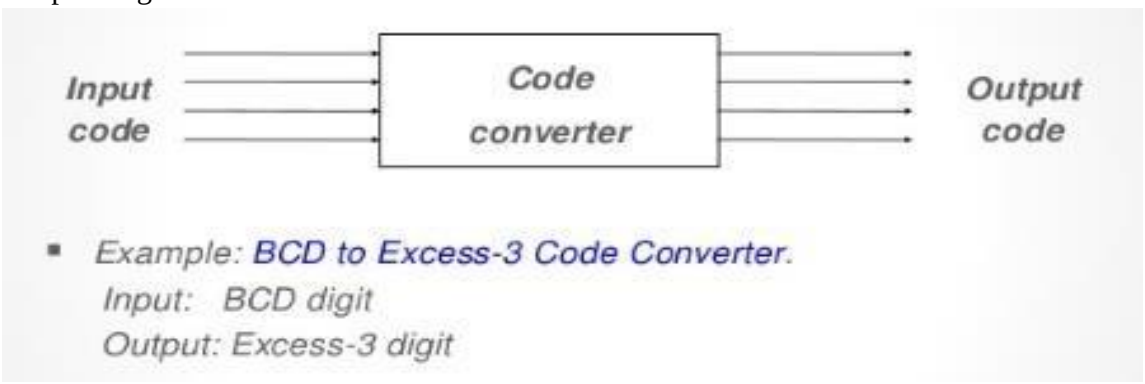
1. Define Demux& Decoder.
2. What are the different methods of indicating active low signals?
3. What is the difference between Demux and Decoder?

B.BCD to Excess-3 code conversion and vice-versa.

COMPONENTS REQUIRED:-

Sl. No	Name of the Component	IC Number
1	EXOR gate	7486
2	Patch chords	
3	Trainer Kit	
4	4 bit parallel adder/subtractor	7483

Theory: Code converter is a combinational circuit that translates the input code word into a new corresponding word.



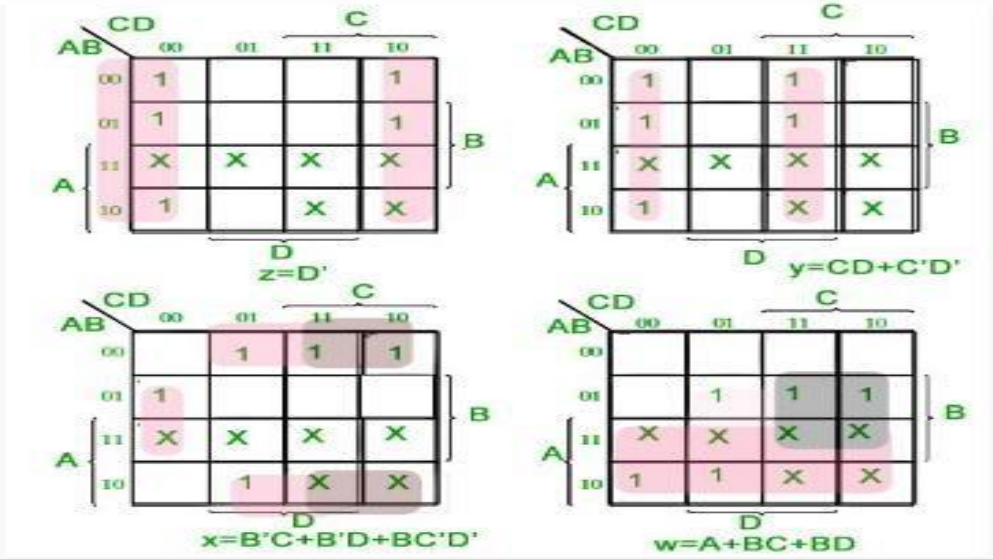
The excess-3 code digit is obtained by adding three to the corresponding BCD digit. To Construct a BCD-to-excess-3-code converter with a 4-bit adder feed BCD-code to the 4-bit adder as the first operand and then feed constant 3 as the second operand. The output is the corresponding excess-3 code. To make it work as a excess-3 to BCD converter, we feed excess-3 code as the first operand and then feed 2's complement of 3 as the second operand. The output is the BCD code.

TRUTH TABLE FOR BCD TO EXCESS -

BCD(8421)				Excess-3			
A	B	C	D	w	x	y	z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

De

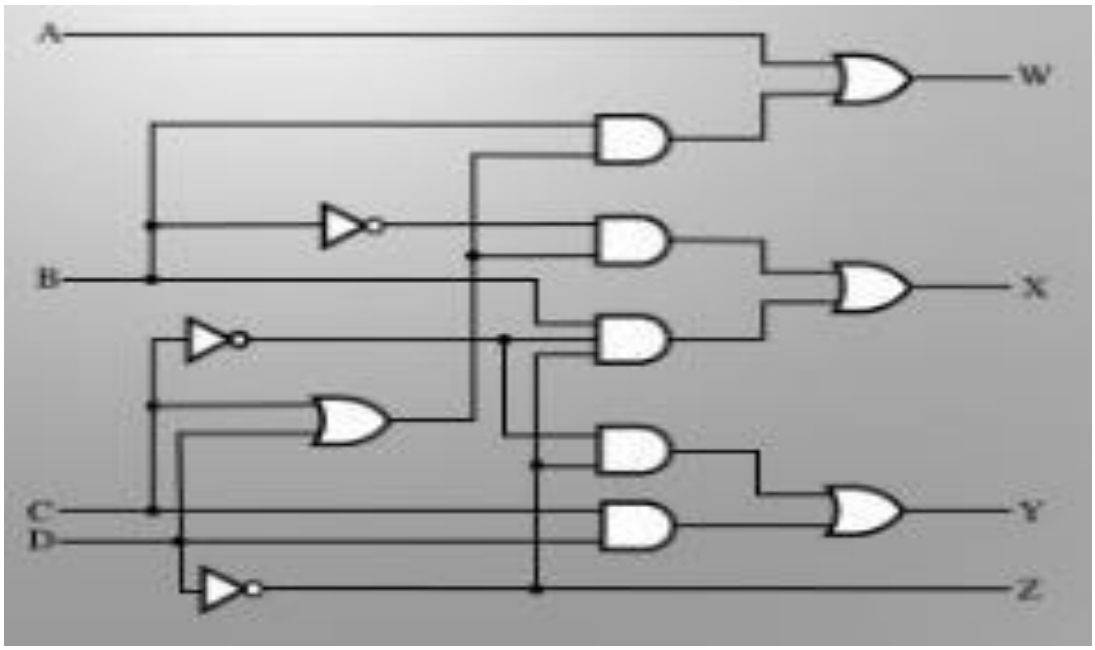
K MAP SIMPLIFICATION:-



Corresponding minimized Boolean expressions for Excess-3 code bits –

$$W = A + BC + BD$$
$$X = \overline{B}C + \overline{B}D + B\overline{C}\,\overline{D}$$
$$Y = CD + \overline{C}\,\overline{D}$$
$$Z = \overline{D}$$

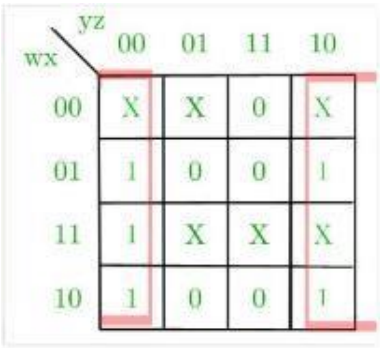
Logic Diagram using Basic Gates:-



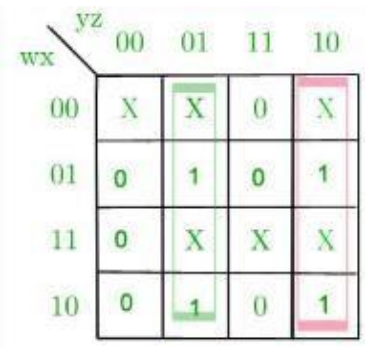
TRUTH TABLE FOR EXCESS – 3 TO BCD:-

Excess-3				BCD			
w	x	y	z	A	B	C	D
0	0	0	0	X	X	X	X
0	0	0	1	X	X	X	X
0	0	1	0	X	X	X	X
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

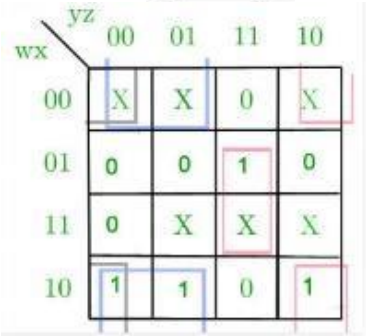
K MAP SIMPLIFICATION:-



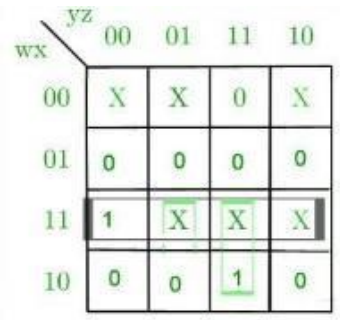
$D = z'$



$C = y'z + yz'$



$B = x'y' + x'z' + xyz$

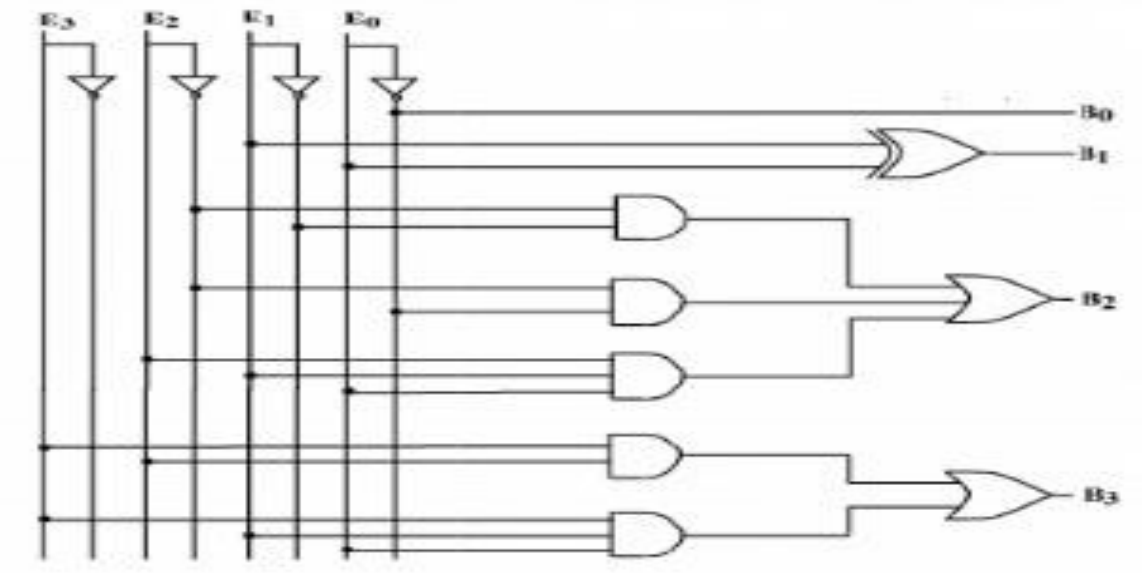


$A = wx + wyz$

Corresponding minimized Boolean expressions for Excess-3 code bits –

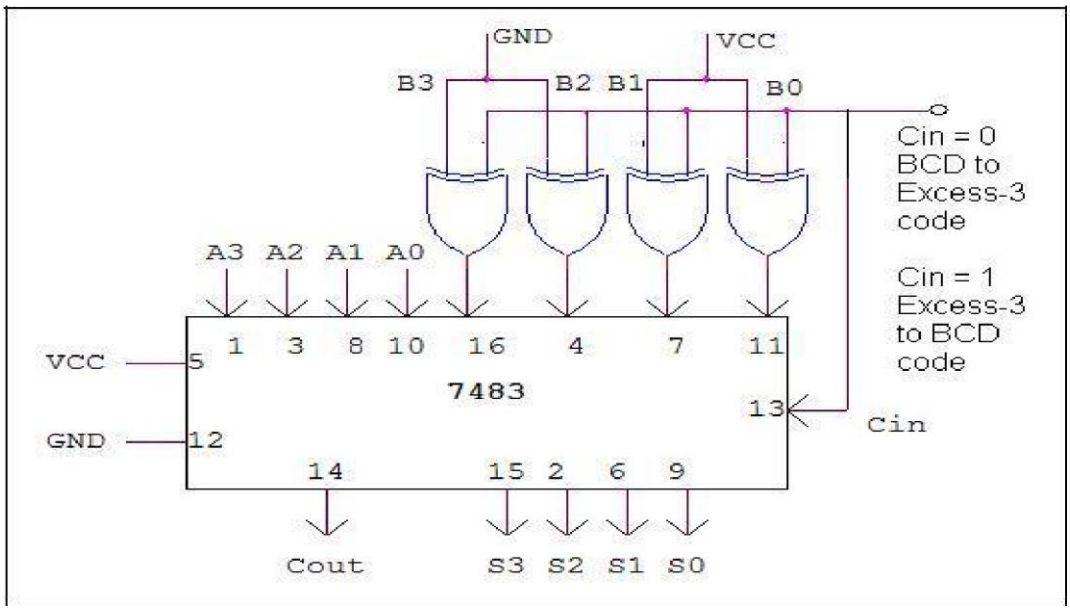
$$A = wx + wyz$$
$$B = x'y' + x'z' + xyz$$
$$C = y'z + yz'$$
$$D = z'$$

W X Y Z



Logic Diagram using Basic Gates:-

Logic Diagram using IC7483 FOR BCD TO EXCESS – 3 & VICE VERSA:-



RESULT: Realized BCD code to Excess-3 code conversion and vice versa using 7483 IC

VIVA QUESTIONS:

1. What are the different methods of representing –ve numbers, which type is preferred and why?
2. Procedure for 1's complement method of subtraction
3. Procedure for 2's complement method of subtraction
4. State different methods of subtraction using complementary methods
5. Why complementary methods are preferred?
6. What are the advantages of 2's complement method?
7. Internal diagram of IC 7483, what is the significance of Cin and Cout pins.
8. Types of Adders, advantages and disadvantages of different types, Explain Look ahead carry adder.
9. What is the internal structure of 7483 IC?
10. What do you mean by code conversion?
11. What are the applications of code conversion?
12. How do you realize a subtractor using full adder?
13. What is a ripple Adder? What are its disadvantages?

7 A .REALIZE USING NAND GATES

VERIFICATION OF MS JK, D & T FLIP-FLOPS

AIM: - Realize Master-Slave JK, D & T Flip-Flops using NAND Gates.

COMPONENTS REQUIRED:-

Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	3 Input NAND gate	7410
2	2 Input NAND gate	7400
3	NOT gate	7404
4	Patch chords	
5	Trainer Kit	

THEORY:

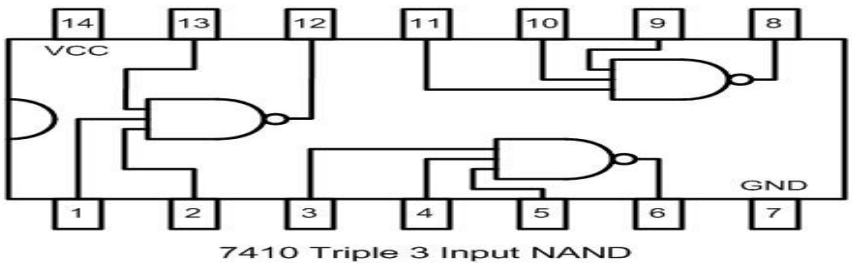
JK flip-flop provides the solution for SR flip-flop problem. Compared to SR flipflop, JK flip flop has two new connections from the Q and Q outputs back to the original input gates. JK flip-flop behaves like the SR flip-flop except for input condition 1 and 1. Its output toggles for every clock pulse input unlike SR flip-flop. Although JK flip-flop circuit is an improvement on the clocked SR flip-flop it still suffers from timing problems called "race". This problem can be solved by Master slave flip-flop.

MS JK Flip Flop: The Master-slave JK flip-flop is basically two JK bitable flip-flops connected together in a series configuration with the outputs form Q and Q' from the slave flip-flop being fed back to the inputs of the Master with the outputs of the Master flip-flop being connected to the two inputs of the slave flip-flop. The circuit accepts input data when the clock signal is "HIGH", and passes the data to the output on the fallingedge of the clock signal. In other words, the Master-Slave JK flip-flop is a "Synchronous" device as it only passes data with the timing of the clock signal. The master slave over comes the race around condition.

T - Flip Flop: MS JK FF is converted to T – FF by shorting J and K inputs. The output of a T – FF changes every time it is triggered at its T – input called Toggle input.

D - Flip Flop: MS JK FF is converted to D – FF by connecting J and K inputs through a NOT gate. The data bit present on the d-input is transferred to the Q – output every time it is clocked.

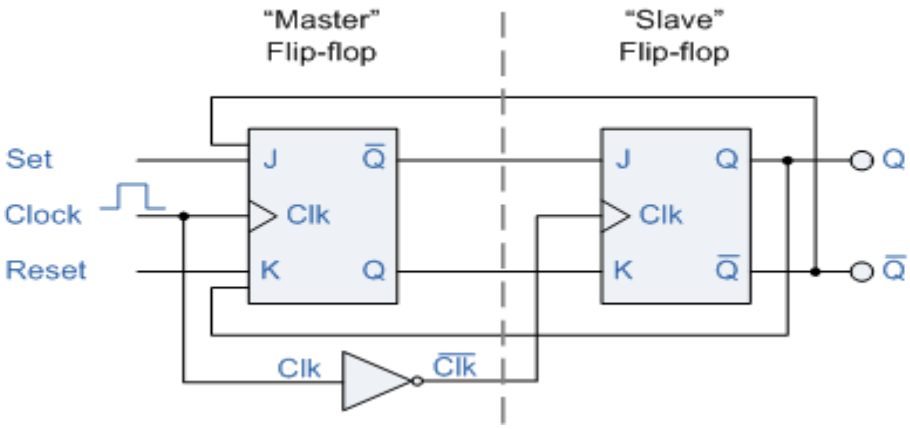
➢ **PIN DETAILS OF 7410:**



7410 Triple 3 Input NAND

i)MASTER-SLAVE JK FLIP-FLOP:

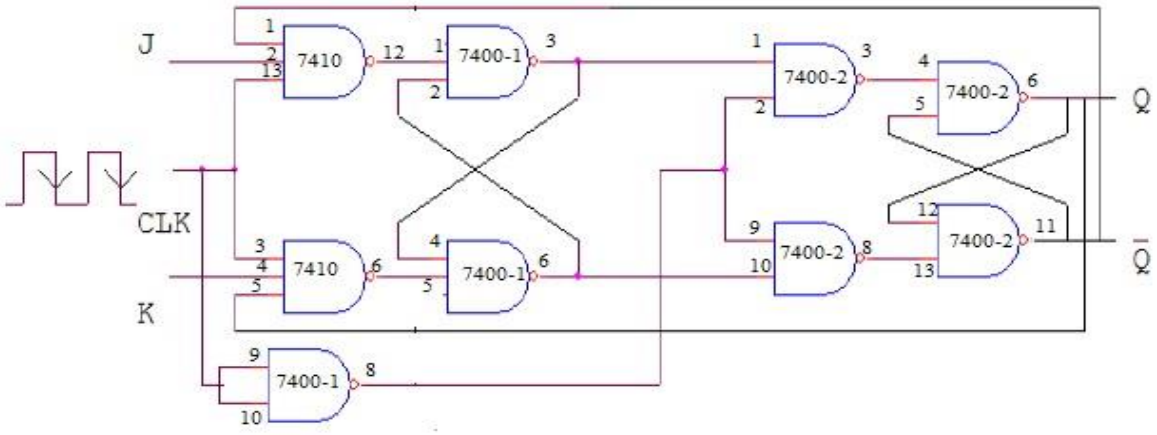
➢ **SYMBOL OF M S-JK FF**



➢ **TRUTH TABLE**:

Clock	J	K	Q+	Q'+	Comment
1	0	0	Q	Q'	No Change
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Q'	Q	Toggle

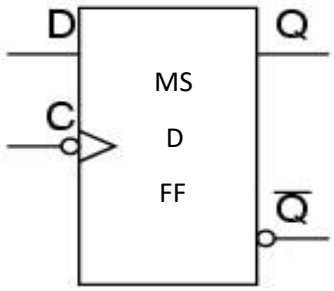
REALIZATION OF MASTER SLAVE J K FLIP FLOP USING NAND GATES:



Logic Diagram of Master Slave J K Flip – Flop Using NAND Gates

ii)MASTER-SLAVE D FLIP-FLOP:

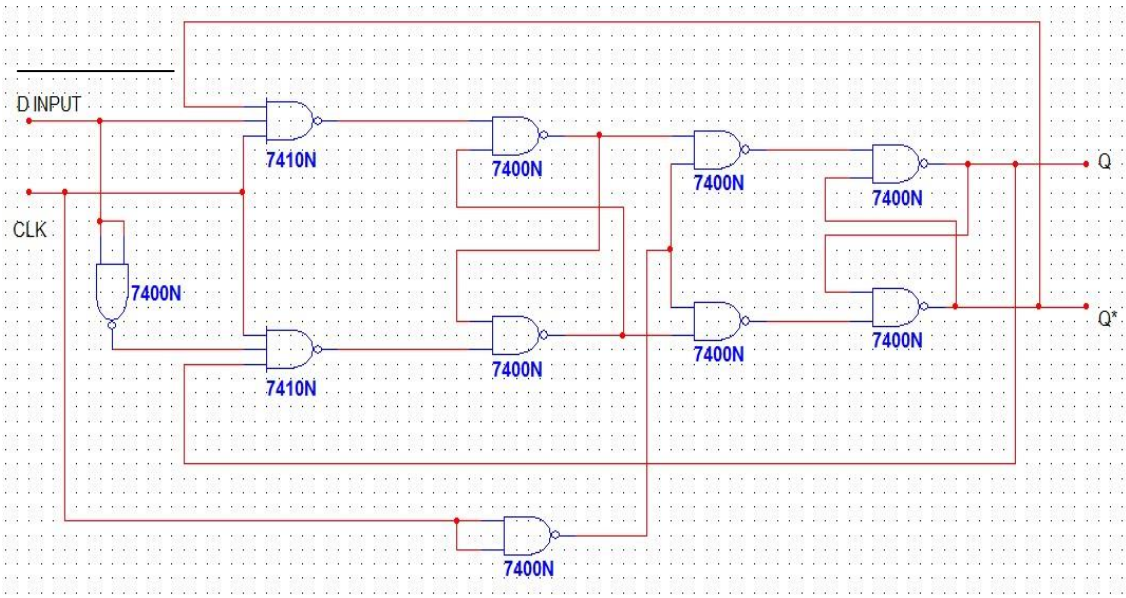
- **SYMBOL OF M S-D FF:**



- **TRUTH TABLE**:

CLK	D	Q^+	$\overline{Q^+}$	Comment
0	X	Q	$\overline{Q}$	No Change
1	0	0	1	Reset
1	1	1	0	Set

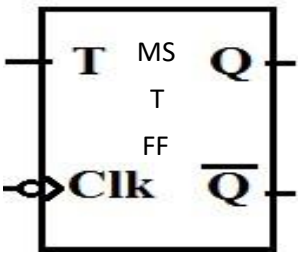
- **REALIZATION OF MASTER SLAVE D FLIP FLOP USING NAND GATES:**



Logic Diagram of Master Slave D Flip – Flop Using NAND Gates

c) MASTER-SLAVE JK FLIP-FLOP:

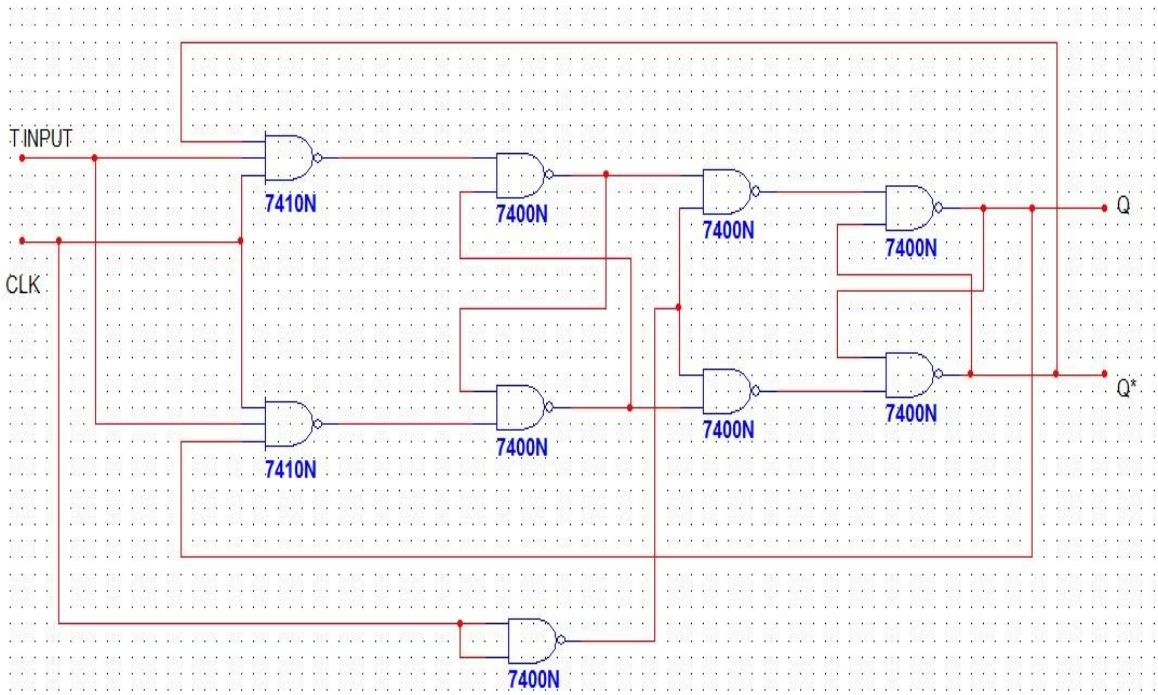
- **SYMBOL OF M S-T FF:**



TRUTH TABLE:

CLK	T	Q^+	$\overline{Q^+}$	Comment
0	X	Q	$\overline{Q}$	No Change
1	0	Q	$\overline{Q}$	No Change
1	1	$\overline{Q}$	Q	Toggle

- **REALIZATION OF MASTER SLAVE T FLIP FLOP USING NAND GATES:**



Logic Diagram of Master Slave T Flip – Flop Using NAND Gates

Procedure:

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in the circuit diagram.
4. Verify the Truth Table and observe the outputs.

Result: Thus the truth table for Master Slave JK FF was verified, D and T FF were realized using MS JK FF.

Viva Questions:

1. Distinguish between the combinational & sequential circuits.
2. What are the two types of sequential circuits?
3. What is a Flip-Flop & Distinguish between the flip-flop & Latch?

4.A Flip-flops is a Divide By _____ Counter.

5. Can we use SR Flip-flops as a D Flip-flops?

7B.Realize the following shift registers using IC7474/IC 7495 (a) SISO (b) SIPO (c) PISO (d) PIPO (e) Ring and (f) Johnson counter.

COMPONENTS REQUIRED:-

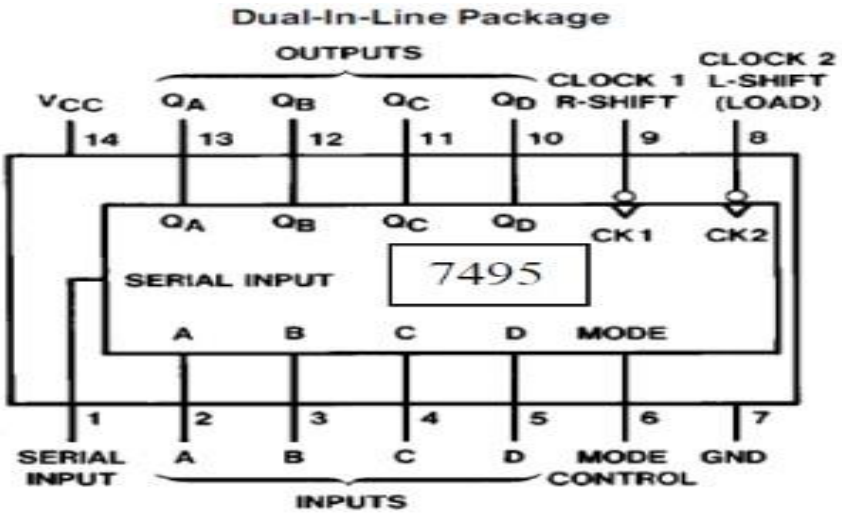
Sl.No	NAME OF THE COMPONENT	IC NUMBER
1 2 3	Shift register Trainer kit Patch Chords	7495

THEORY:

A Shift register is a storage device that can be used for temporary storage of binary data he basic building block in all shift registers is the flip-flop, mainly a D-type flip-flop. Based on the method by which data can be loaded onto and read from shift registers, they are classified. The IC 7495 is a 4-bit shift registers, allowing

- Serial in serial out (SISO)
- Serial in parallel out (SIPO)
- Parallel in serial out (PISO)
- Parallel in parallel out (PIPO) above all four are shift right operation and also can do Shift left operation.

PIN DIAGRAM OF IC 7495:



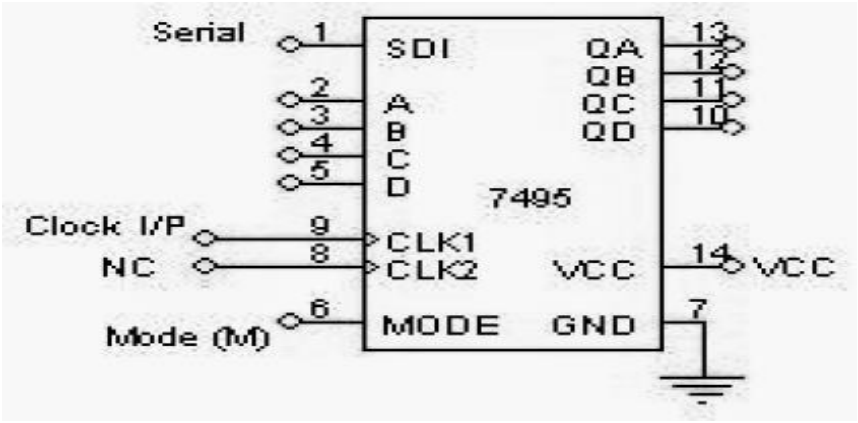
- A, B, C and D : Parallel Data Inputs of shift register
- Q_A, Q_B, Q_C and Q_D : Parallel Data Output of shift register
- Mode SER = Serial Data Input
- CK1: Loading Serial Input Data, for shift right.
- CK2: Loading Parallel Input Data, for shift left .

- M = Mode Control: 1/0
- (If M= 1, CK2 is enabled, M= 0, CK1 is enabled)

a)SERIAL IN SERIAL OUT (SISO):

The input applied is in serial form as and the Clk pulse is applied at the data moves by one position for every single Clk Input and the output obtained is in the serial form from the 4th pulse.

- **LOGIC DIAGRAM OF SISO:**



TRUTH TABLE FOR SISO:

Clock	Serial i/p	QA	QB	QC	QD
1	do=0	0	X	X	X
2	d1=1	1	0	X	X
3	d2=1	1	1	0	X
4	d3=1	1	1	1	0=do
5	X	X	1	1	1=d1
6	X	X	X	1	1=d2
7	X	X	X	X	1=d3

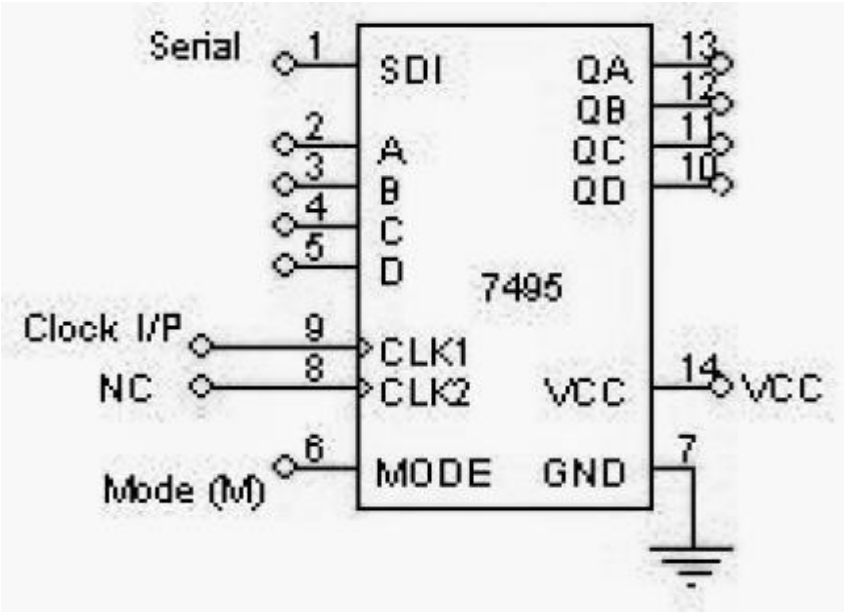
Procedure

1. Connections are made as per logic diagram.
2. Load the shift register with 4 bits of data one by one serially.
3. At the end of 4th clock pulse the first data ‘d0’ appears at QD.
4. Apply another clock pulse; the second data ‘d1’ appears at QD.
5. Apply another clock pulse; the third data appears at QD.
6. Application of next clock pulse will enable the 4th data ‘d3’ to appear at QD. Thus the data applied serially at the input comes out serially at QD

b) SERIAL IN PARALLEL OUT (SIPO):

Data is applied at the serial input and the output is obtained in the parallel form after full data word has been shifted.

- **LOGIC DIAGRAM OF SIPO:**



- **TRUTH TABLE FOR SIPO:**

Clock	Serial i/p	QA	QB	QC	QD
1	0	0	X	X	X
2	1	1	0	X	X
3	1	1	1	0	X
4	1	1	1	1	0

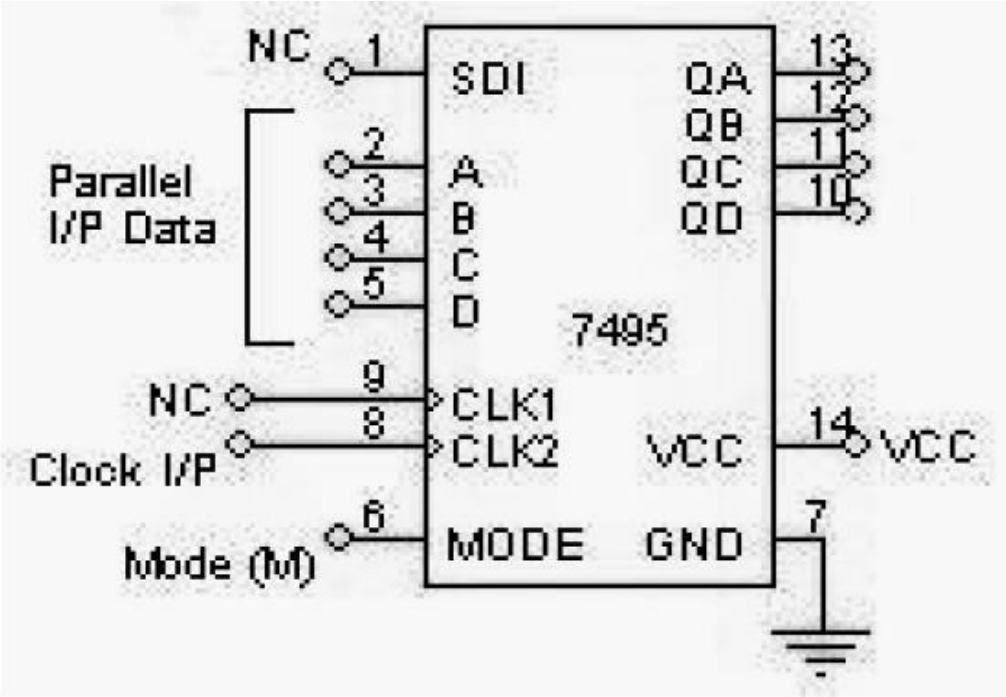
Procedure

1. Connections are made as per logic diagram.
2. Apply the data at serial i/p
3. Apply one clock pulse at clock 1 (Right Shift) observe this data at QA.
4. Apply the next data at serial i/p.
5. Apply one clock pulse at clock 2, observe that the data on QA will shift to QB and the new data applied will appear at QA.
6. Repeat steps 2 and 3 till all the 4 bits data are entered one by one into the shift register.

c) PARALLEL IN SERIAL OUT (PISO):

Data is loaded in parallel and can be shifted out in serial form.

- **LOGIC DIAGRAM OF P ISO:**



- **TRUTH TABLE FOR P ISO:**

Mode	Clock	Parallel i/p				Parallel o/p ↓ SERIAL			
		A	B	C	D	QA	QB	QC	QD
1	1	1	0	1	1	1	0	1	1
0	2	X	X	X	X	X	1	0	1
0	3	X	X	X	X	X	X	1	0
0	4	X	X	X	X	X	X	X	1

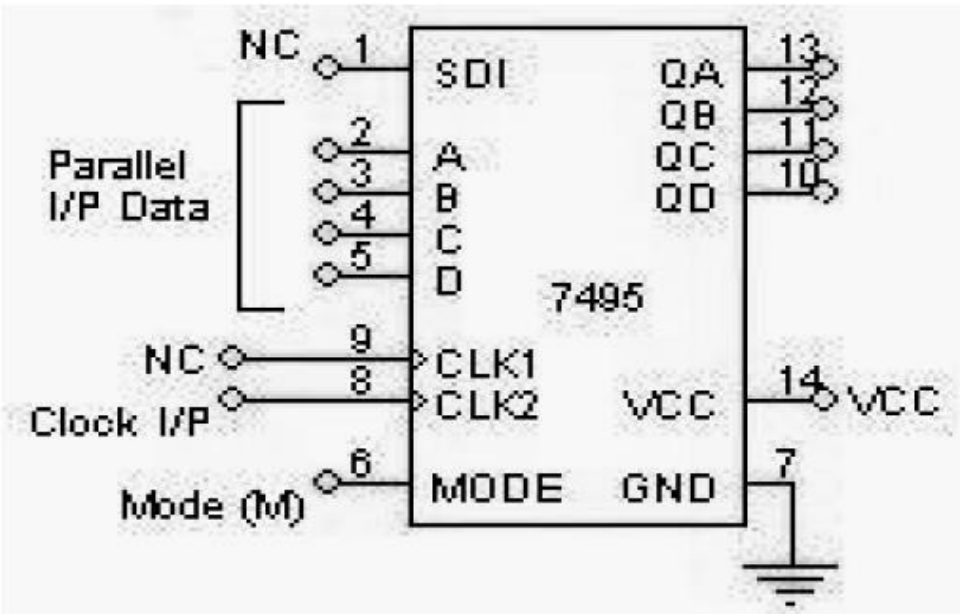
Procedure

1. Connections are made as per logic diagram.
2. Apply the desired 4 bit data at A, B, C and D.
3. Keeping the mode control M=1 apply one clock pulse. The data applied at A, B, C and D will appear at QA, QB, QC and QD respectively.
4. Now mode control M=0. Apply clock pulses one by one and observe the data coming out serially at QD.

d) PARALLEL IN PARALLEL OUT (PIPO):

Data is loaded in parallel and read out in parallel form.

- **LOGIC DIAGRAM OF PIPO:**



- **TRUTH TABLE FOR PIPO:**

Clock	Parallel i/p				Parallel o/p			
	A	B	C	D	QA	QB	QC	QD
1	1	0	1	1	1	0	1	1

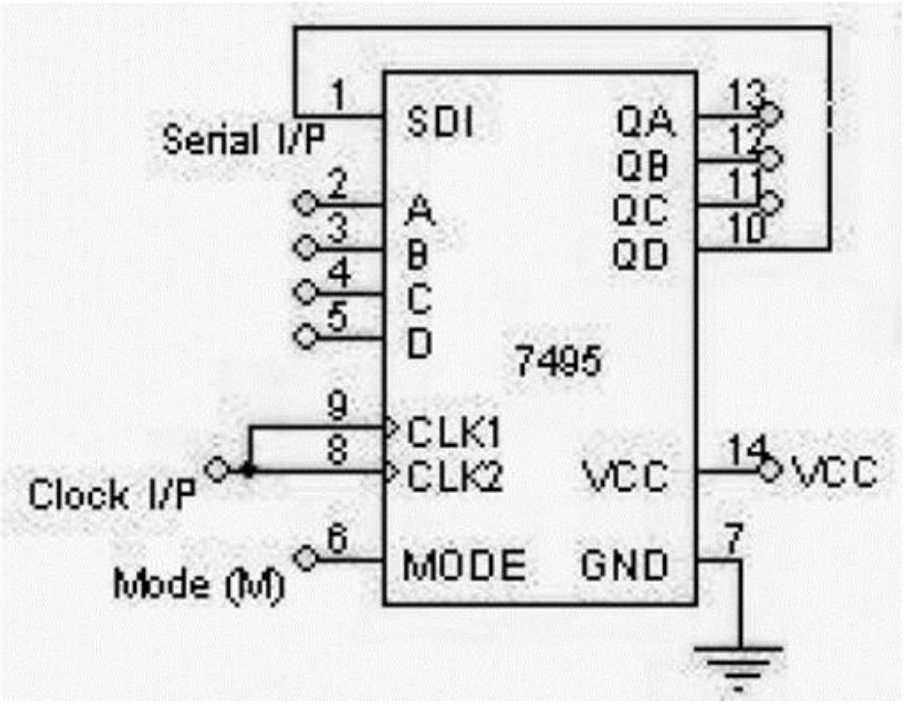
Procedure

1. Connections are made as per logic diagram.
2. Apply the 4 bit data at A, B, C and D.
3. Apply one clock pulse at Clock 2 (Note: Mode control M=1).
4. The 4 bit data at A, B, C and D appears at QA, QB, QC and QD respectively.

e)RING COUNTER:

Ring counter is also called as shift register counter where the FF^{1}S are coupled as in a shift register and the last FF is coupled back to the first ,which gives the array of ff ′ the shape of ring . Counting sequence of such counter will depend upon initial state, the desired initial state should provided by parallel loading before counting begin, loading can be done by placing a single '1' or single '0' for allowed counting sequence. The logic '1' or '0' will advance by one flip-flop around the ring for each clk pulse and return to original FF after exactly four clk pulses as there are 4FF , the standard ring counter requires n FF's to derive a modulo (n+1) counter.

LOGIC DIAGRAM OF RING COUNTER:



- **TRUTH TABLE FOR RING COUNTER:**

Mode	Clock	QA	QB	QC	QD
1	1	1	0	0	0
0	2	0	1	0	0
0	3	0	0	1	0
0	4	0	0	0	1
0	5	1	0	0	0
0	6	repeats			

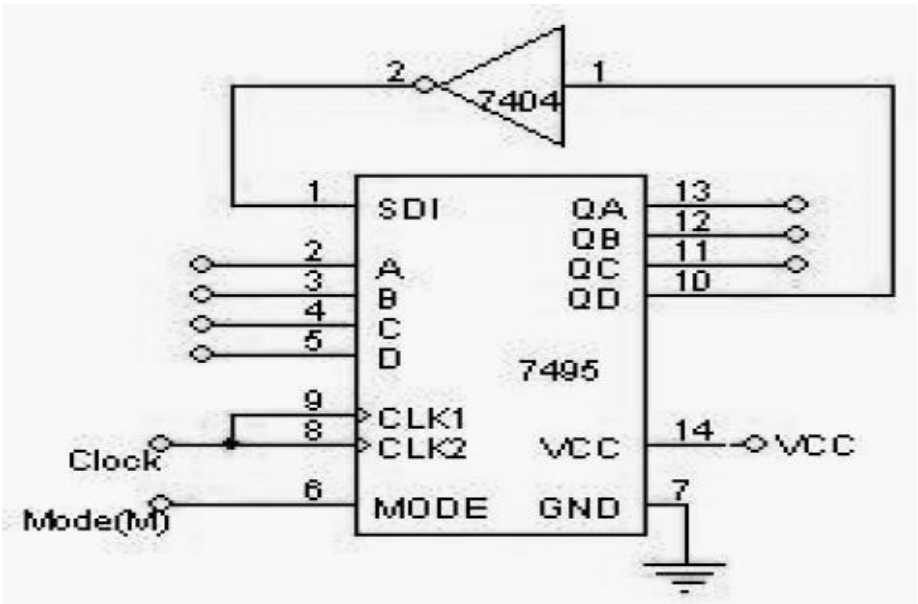
PROCEDURE:

1. Connections are made as per the logic diagram.
2. Apply the data 1000 at A, B, C and D respectively.
3. Keeping the mode M = 1, apply one clock pulse.
4. Now the mode M is made 0 and clock pulses are applied one by one and the truth table is verified.

f) JOHNSON RING COUNTER:

Johnson counter is similar to ring counter that the complement of the output of last stage is connected to the input of first stage therefore it is called as twisted ring counter .it requires n/2 FF,s for a modulo n counter.

- **LOGIC DIAGRAM OF JOHNSON RING COUNTER:**



- **TRUTH TABLE FOR JOHNSON RING COUNTER:**

Mode	Clock	QA	QB	QC	QD
1	1	1	0	0	0
0	2	1	1	0	0
0	3	1	1	1	0
0	4	1	1	1	1
0	5	0	1	1	1
0	6	0	0	1	1
0	7	0	0	0	1
0	8	0	0	0	0
0	9	1	0	0	0
0	10	repeats			

PROCEDURE:

1. Connections are made as per the logic diagram.
2. Apply the data 1000 at A, B, C and D respectively.
3. Keeping the mode M = 1, apply one clock pulse.
4. Now the mode M is made 0 and clock pulses are applied one by one and the truth table is verified.

RESULT: All the outputs are verified with the truth table.

8. Realize

(a) Design Mod – N Synchronous Up Counter & Down Counter using 7476

(b) Mod-N Counter using IC7490 / 7476

(c) Synchronous counter using IC74192

COMPONENTS REQUIRED:-

Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	Decade Counter (Asynchronous Counter)	7490
2	Decade UP/DOWN Counter (Synchronous Counter)	7476
3	Patch chords	74192
4	Trainer Kit	

THEORY:

A sequential circuit that gives through a prescribed sequence of states upon the application of input pluses is called counters. The straight binary sequence counter is the simple and most straight forward. An n-bit binary counter has n flip-flops and can count in binary from 0 to 2^n -1.

- **Asynchronous counter:**

A binary ripple (Asynchronous) counter consists of series connections of T- flip-flops without any logic gates. Each FF is triggered by the output of its preceding FF goes from 1 to 0.

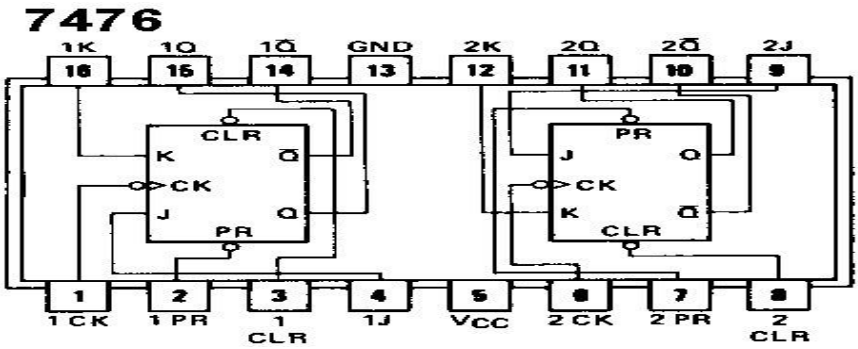
- **Synchronous Counter:**

In Synchronous counters all FF are triggered simultaneously by the count pluse. The FF is complemented only if its T input is equal to 1 the advantage of synchronous counter is its speed, it takes only one propagation delay time for the correct binary count to appear the clock edge bits.

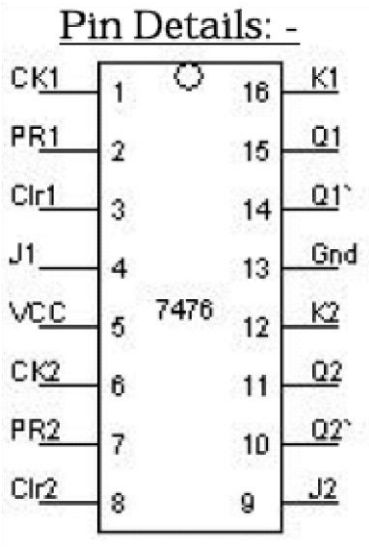
IC 7490 is a Divide-by 10 counter using 4 Master slave JK flip-flops. It contains a Divide-by 2 and Divide-by 5 counters, which can be cascaded to give a Divide-by 10 counter and The IC 74LS192 is an UP/DOWN BCD Decade (8421) Counter.

(a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flipflop:-

- **Internal Diagram of IC 7490:**



- **Pin Diagram of IC 7476:**



Notes & observation:

- Each 7476 IC has two J –K flip flops (FFs) since we are dealing with 3 bit counters, 3 FFs are needed. So. 2 – 7476 IC's are used.
- J and K I/Ps of FFs may be connected to logic '1' or keep it open to operate the FF's in toggle mode.
- When Pr='1', Cr = '0', counter is cleared, $Q_o = Q_1 = Q_2 = 0$ When Pr='0', Cr = '1', counter is preset, $Q_o = Q_1 = Q_2 = 1$

Keep Pr='1', Cr = '1', for count mode.

- **DESIGN OF 3-BIT SYNCHRNOUS UP COUNTER (MOD 8 COUNTERS): ➢TRUTH TABLE:**

Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Present count			Next count		
Q_C	Q_B	Q_A	Q_C	Q_B	Q_A
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

JK FF EXCITATION TABLE:

Q	Q+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

DESIGN:

1	X	X	1
1	X	X	1

$J_A = 1$

X	1	1	X
X	1	1	X

$K_A = 1$

0	1	X	X
X	1	X	X

$J_B = Q_A$

X	X	1	0
X	X	1	0

$K_B = Q_A$

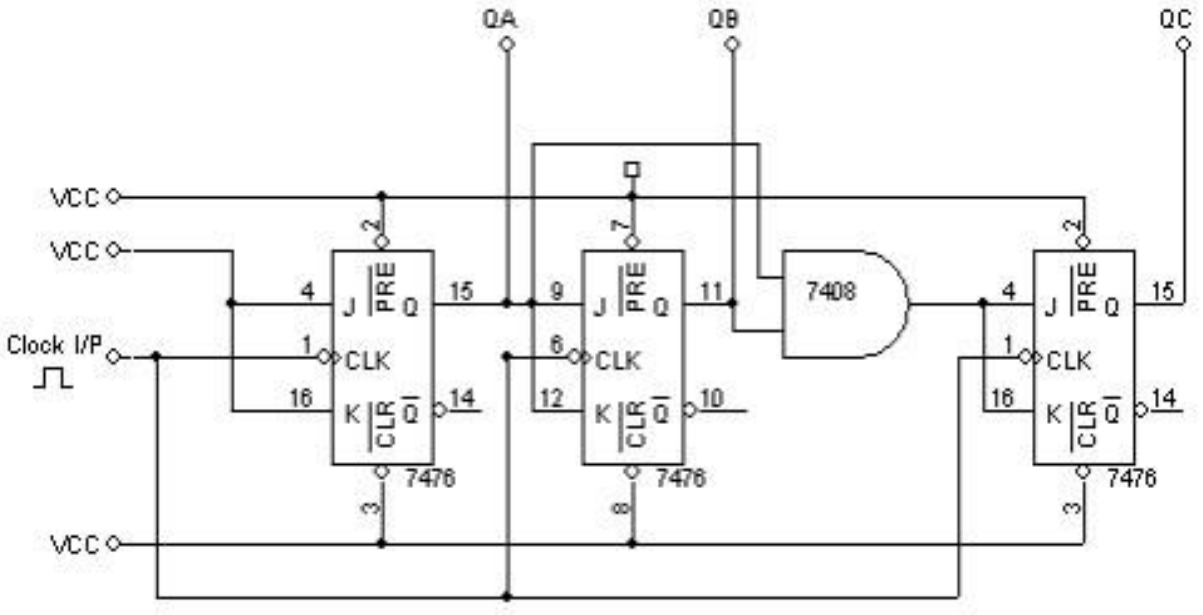
0	0	1	0
X	X	X	X

$J_C = Q_B Q_A$

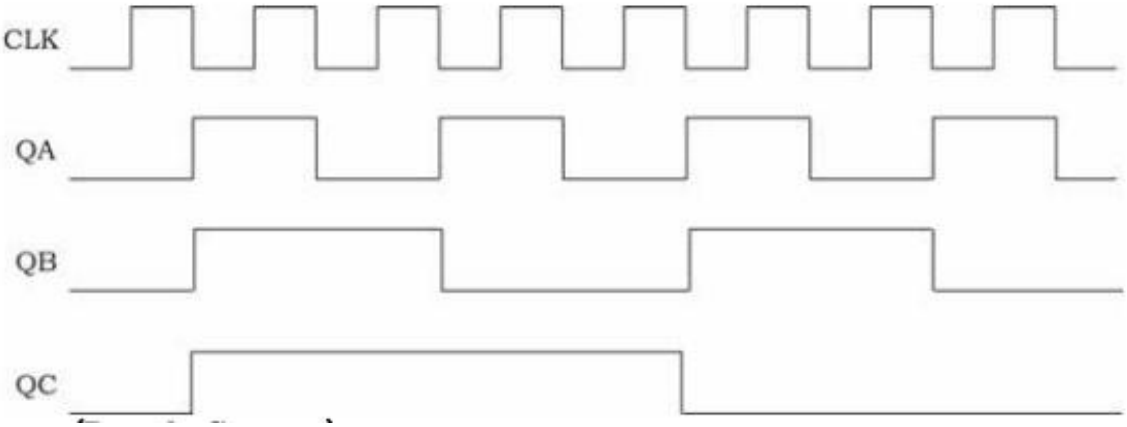
X	X	X	X
0	0	1	0

$K_C = Q_B Q_A$

LOGIC DIAGRAM OF 3-BIT SYNCHRNOUS UP COUNTER USING IC 7476:



TIMING DIAGRAM:



- **LOGIC DIAGRAM OF 3-BIT SYNCHRNOUS DOWN COUNTER USING IC 7476:**

- **TRUTH TABLE:**

CLOCK	Q2	Q1	Q0
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0

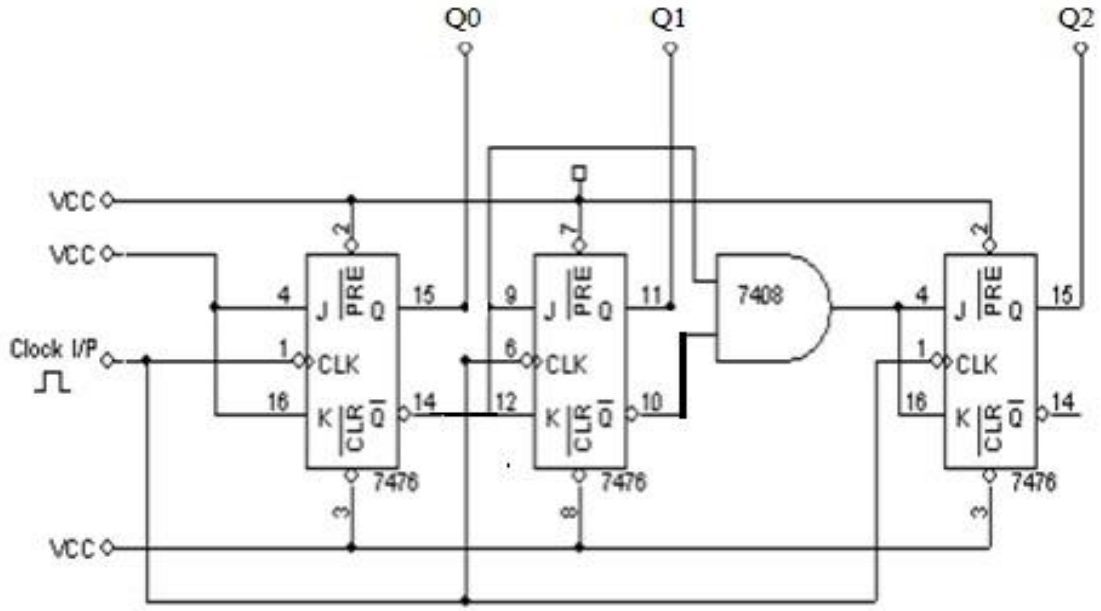
Present State	Next State	J_2K_2	J_1K_1	J_0K_0
000	111	1 d	1 d	1 d
001	000	0 d	0 d	d 1
010	001	0 d	d 1	1 d
011	010	0 d	d 0	d 1
100	011	d 1	1 d	1 d
101	100	d 0	0 d	d 1
110	101	d 0	d 1	1 d
111	110	d 0	d 0	d 1

- **DESIGN:**

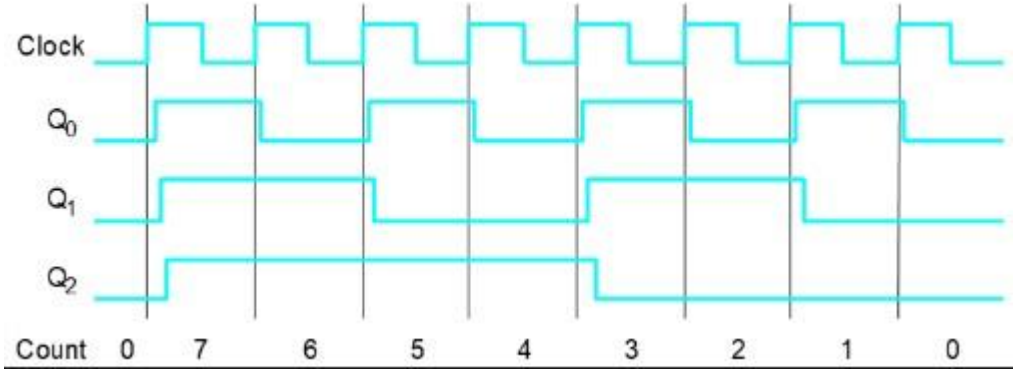
Simplify using K- MAP

- J_0& $K_0 = 1$
- J_1& $K_1 = Q_0$
- J_2& $K_2 = Q_1 Q_0$

LOGIC DIAGRAM OF 3-BIT SYNCHRNOUS DOWN COUNTER USING IC 7476:

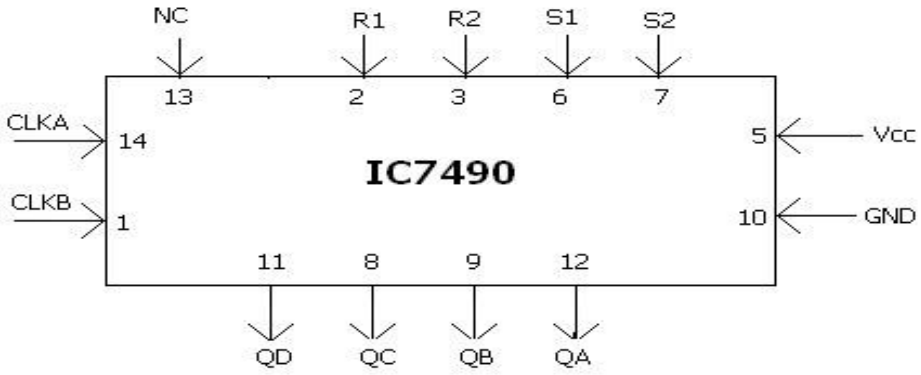


- **TIMING DIAGRAM:**

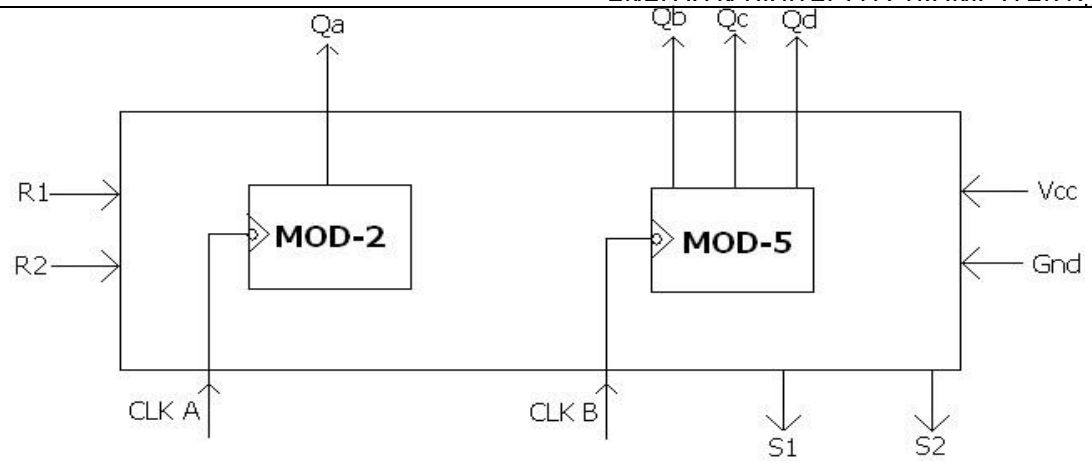


(ii) Mod-N Asynchronous Counter using IC7490:

- **PIN DIAGRAM OF IC 7490:**



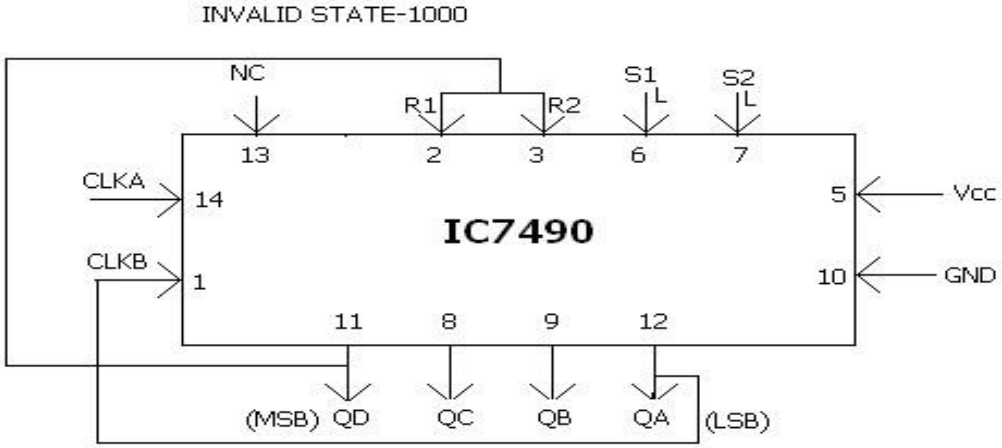
INTERNAL DIAGRAM OF IC 7490:



- **Conditional Table:**

R1	R2	S1	S2	Q_a	Q_b	Q_c	Q_d
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	L	H	H	1	0	0	1
L	X	L	X	MOD-2 COUNTER			
X	L	X	L	MOD-5 COUNTER			
L	L	L	L	MOD-10 COUNTER			

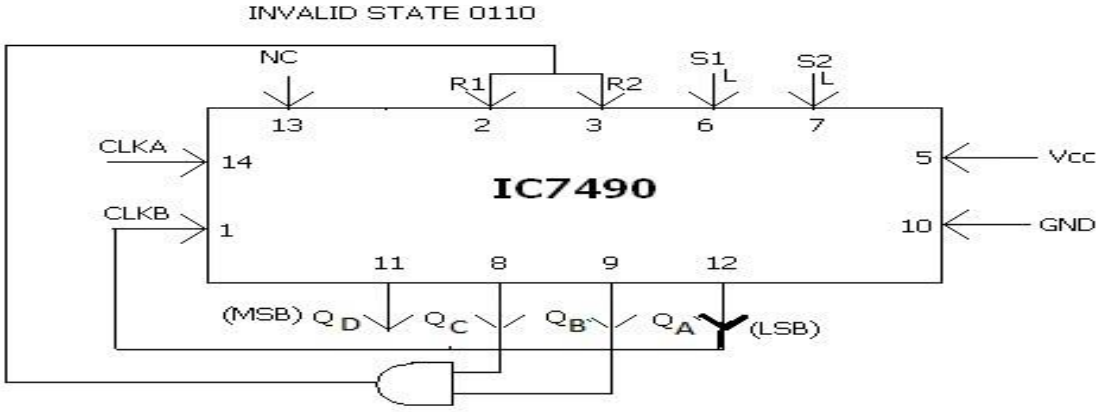
LOGIC DIAGRAM OF MOD-8 COUNTER USING IC 7490 :



- **TRUTH TABLE:**

Clock	QD	QC	QB	QA
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	0	0	0	0

- **LOGIC DIAGRAM OF MOD-6 COUNTER USING IC 7490**



- **TRUTH TABLE:**

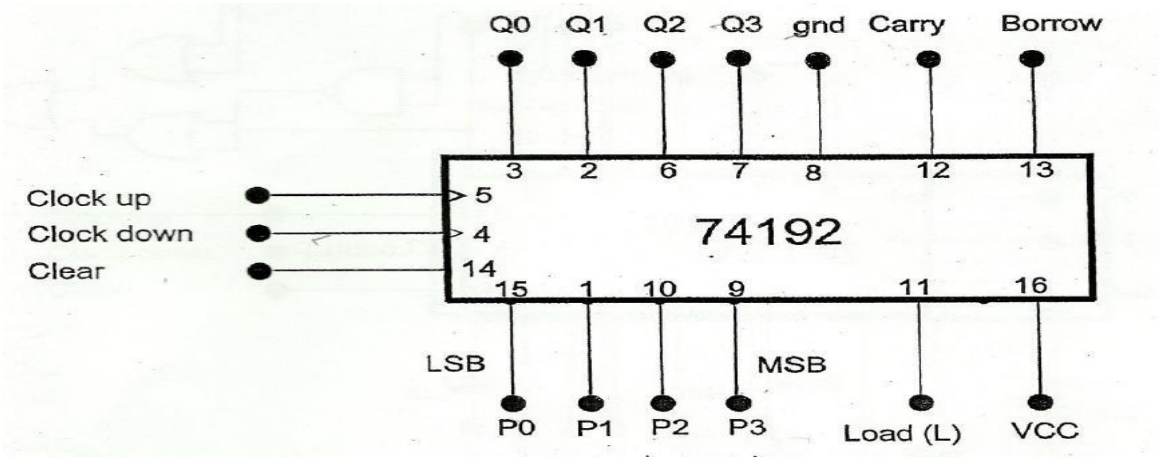
CLOCK	QD	QC	QB	QA
0	**0**	**0**	**0**	**0**
1	**0**	**0**	**0**	**1**
2	**0**	**0**	**1**	**0**
3	**0**	**0**	**1**	**1**
4	**0**	**1**	**0**	**0**
5	**0**	**1**	**0**	**1**
6	**0**	**0**	**0**	**0**

PROCEDURE:

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in the logic diagram.
4. Verify the Truth Table and observe the outputs.

(iii)Mod-N Synchronous counter using IC74192:

- **PIN DIAGRAM OF IC 74192:**

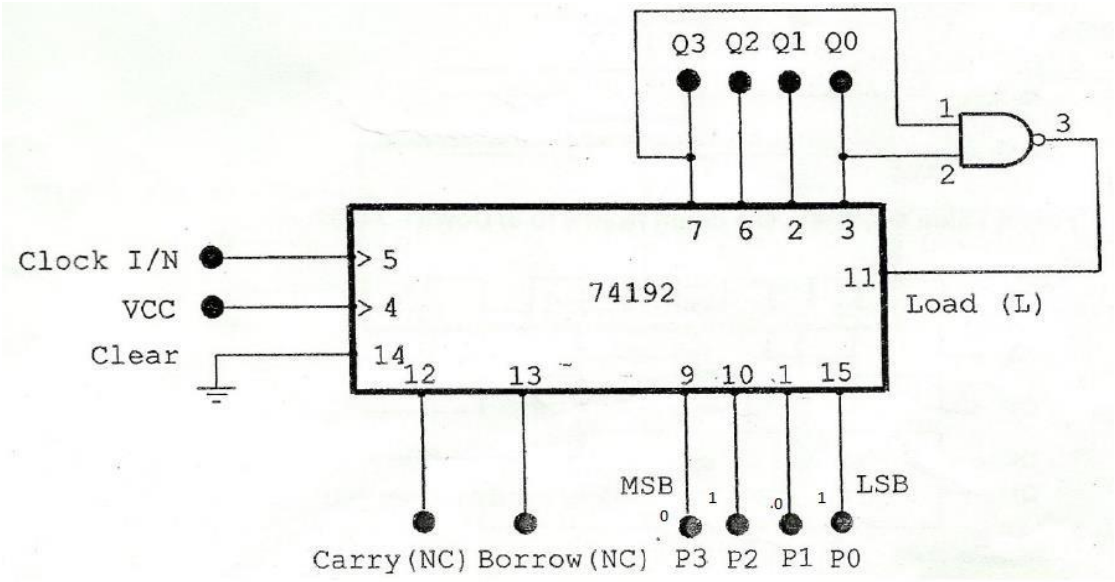


Note: Carry and borrow are mainly used for cascading the counters.

- **FUNCTION TABLE:**

Load	Clear	Clk-up	Clk-down	Mode
X	1	X	X	Reset to zero
1	0	↑	1	Up-count
1	0	1	↑	Down-count
0	0	X	X	Preset
1	0	1	1	Stop count

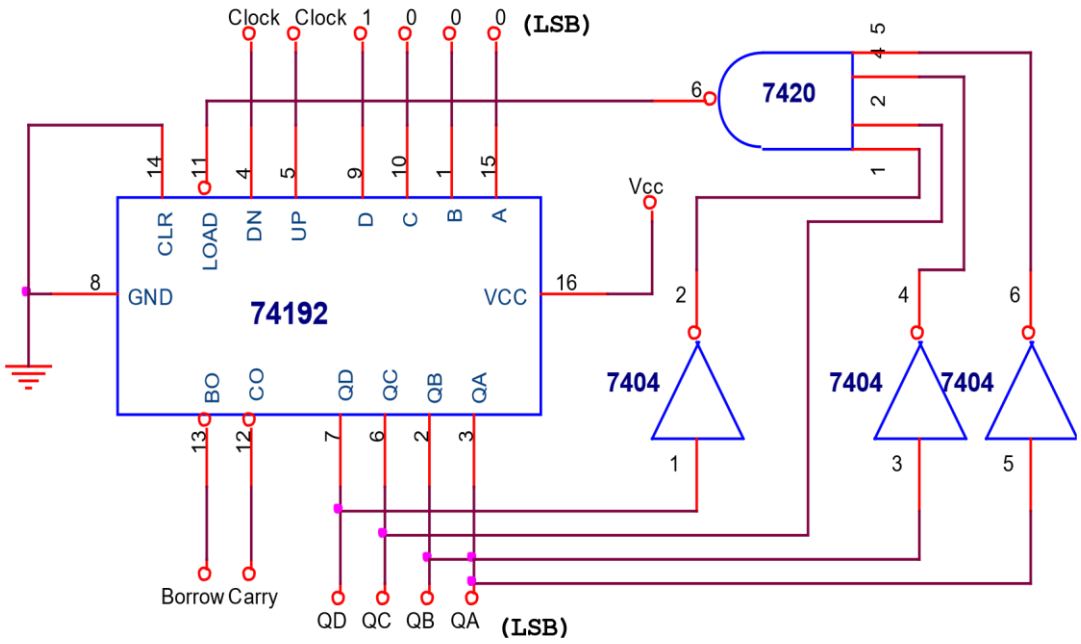
- **<u>LOGIC DIAGRAM OF IC 74192 AS PRE-SETTABLE UP COUNTER TO COUNT FROM 5 TO 8 (Preset Value = 5 & N= 4) :</u>**



- **TRUTH TABLE:**

Clock	QD	QC	QB	QA
1	0	1	0	1
2	0	1	1	0
3	0	1	1	1
4	1	0	0	0
5	0	1	0	1

- **LOGIC DIAGRAM OF IC 74192 AS PRE-SETTABLE DOWN COUNTER TO COUNT FROM 8 TO 5 (Preset Value = 8 & N= 4) :**



TRUTH TABLE:

CLK	Q_D	Q_C	Q_B	Q_A
0	1	0	0	0
1	0	1	1	1
2	0	1	1	1
3	0	1	0	1
4	1	0	0	0

PROCEDURE:

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in the logic diagram.
4. Verify the truth Table and observe the outputs.

Result: Thus the modulo counter using IC 7490 & IC 74192 were designed, constructed and verified.

Viva Questions:

1. Define MOD of a counter?
2. What is a difference between a Synchronous & Asynchronous Counters?
3. Name the IC's which are used as a Synchronous Counters?
4. Define Triggering in the Counters?

9.Design 4 bit R–2R Op-Amp Digital to Analog Converter

AIM:To verify the working of R-2R DAC for Vref=5V .

Components :

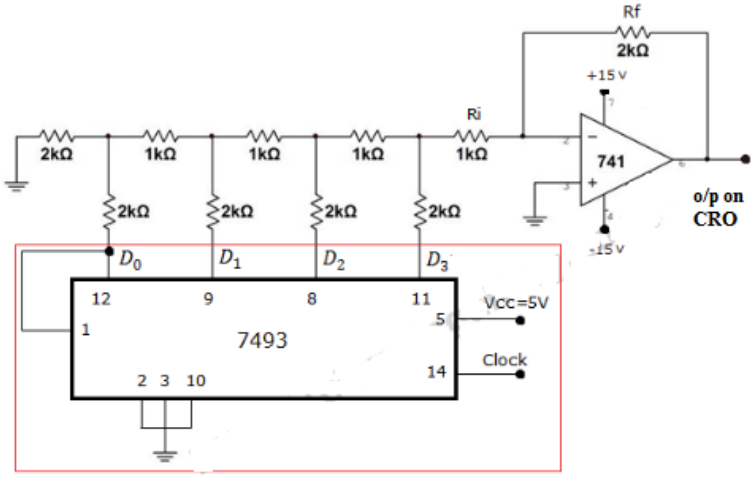
Sl.No	Particulars	Specification	Quantity
1	OP AMP	uA741	01
2.	Resistors	as per design	as per design
3.	IC 7493	-	01

Theory:

In electronics, a Digital-to-Analog converter (DAC, D/A, D–A, D2A, or D-to-A) is device that converts a digital signal into an analog signal. An analog-to-digital converter (ADC) performs the reverse function. DACs are commonly used in music players to convert digital data streams into analog audio signals. They are also used in televisions and mobile phones to convert digital video data into analog video signals which connect to the screen drivers to display monochrome or color images.

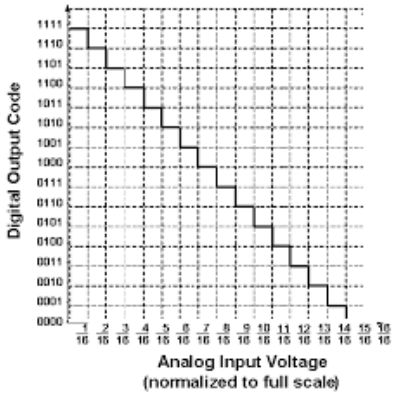
An R–2R Ladder is a simple and inexpensive way to perform digital-to-analog conversion, using repetitivethe non-repetitive reference network.arrangements of precise resistor networks in a ladder-like configuration. In a basic R–2R resistor ladder network Bit a1 (most significant bit, MSB) through bit a0 (leastsignificant bit, LSB) are driven from digital logic gates. Ideally, the bit inputs are switched between V = 0 (logic 0) and V =Vref(logic1).TheR–2Rnetworkcausesthesedigitalbitstobeweightedintheircontributiontotheoutput voltage Vout. Depending on which bits are set to 1 and which to 0, the output voltage (Vout) will have a corresponding stepped value between 0 andVref minus the value of the minimal step, corresponding to bit.The actual value of Vref(and the voltage of logic 0) will depend on the type of technology usedtogenerate the digital signals.

Circuit Diagram:



In this circuit the 7493 IC simply provides digital inputs to DAC. It is a counter IC and not an integral part of the DAC circuit. You can apply any combinations of binary inputs to $D_3D_2D_1D_0$.

Output Waveform



Design: Design a 4 bit R-2R DAC for an O/P voltage of 5 V when the input is $D_oD_1D_2D_3$

$V_0 = -\frac{R_f V_{ref}}{R}\left[\frac{D_3}{2}+\frac{D_2}{4}+\frac{D_1}{8}+\frac{D_0}{16}\right]$, Assume R_f=2R and R = 10K , V_{ref}=5V

Observation:

Decimal Value	Binary Inputs				Analog O/P V_o(volts) Theoretical values	Analog O/P Vo(volts) Practical values (Multimeter/CRO Reading)
	D3 (MSB)	D2	D1	D0 (LSB)		
0	0	0	0	0		
1	0	0	0	1		
2	0	0	1	0		
3	0	0	1	1		
4	0	1	0	0		
5	0	1	0	1		
6	0	1	1	0		
7	0	1	1	1		
8	1	0	0	0		
9	1	0	0	1		
10	1	0	1	0		
11	1	0	1	1		
12	1	1	0	0		
13	1	1	0	1		
14	1	1	1	0		
15	1	1	1	1		

Procedure:

0. Connections are made as shown in the circuitdiagram.
1. Digital input data is given at D_3, D_2, D_1, D_0 and corresponding analog output voltage V0 ismeasured.
2. The designed values areverified.

Result:

Practical values are calculated and compared with theoretical values

Viva Questions

1. Mention different types of digital to analog converters
2. Describe types of analog to digital converters
3. List out differences between R2R and successive approximation converter.

10.SEQUENCE GENERATOR

AIM: Design Pseudo Random Sequence generator using 7495.

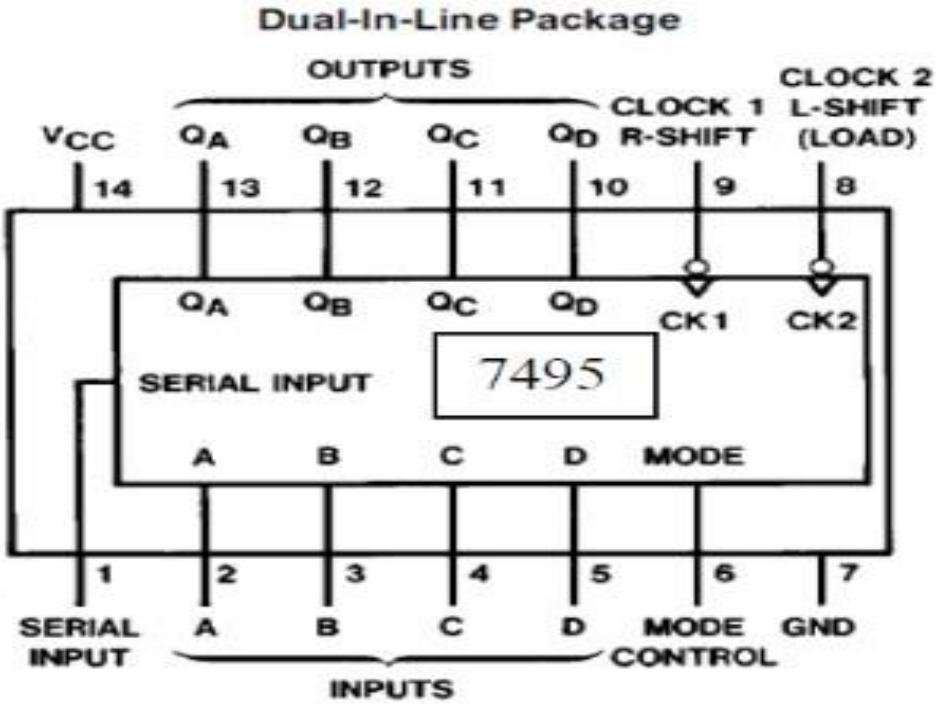
COMPONENTS REQUIRED:-

Sl.No	NAME OF THE COMPONENT	IC NUMBER
1	Shift register	7495
2	ExOR	7486
3	Trainer Kit	
4	Patch Chords	

THEORY:.

Sequence generator which generates a prescribed sequence of bits in synchronous with a clock is referred to as a Sequence generater.Shift register with feedback can be used as sequence generator on waveform generator. A circuit which generates a prescribed sequence of bits in synchronism with a clock is called as sequence generator. The output Y of the next state decoder is function of Qn-1, Qn-2… Q1, Q0. This system similar to ring counter. Y = Q0 or a twisted ring counter (Y = Q0bar) which are special cases of sequence generator. In order to build a sequence generator, capable of generating a sequence of length S, it is necessary to use a minimum **n** number of Flip Flops where **n** satisfies the condition, **$S <= 2^n - 1$.**

- **PIN DIAGRAM OF IC 7495:**



- A, B, C and D : Parallel Data Inputs of shift register
- Q_A, Q_B, Q_C and Q_D : Parallel Data Output of shift register
- Mode SER = Serial Data Input
- CK1: Loading Serial Input Data, for shift right.
- CK2: Loading Parallel Input Data, for shift left .
- M = Mode Control: 1/0 (If M= 1, CK2 is enabled, M= 0, CK1 is enabled)

- **Design of the sequence generator for the sequence S = 100010011010111. As length of S = 15. Hence we require at least 4 Flip Flops**

- **TRUTH TABLE:**

Q_A	Q_B	Q_C	Q_D	Y
1	1	1	1	0
0	1	1	1	0
0	0	1	1	0
0	0	0	1	1
1	0	0	0	0
0	1	0	0	0
0	0	1	0	1
1	0	0	1	1
1	1	0	0	0
0	1	1	0	1
1	0	1	1	0
0	1	0	1	1
1	0	1	0	1
1	1	0	1	1
1	1	1	0	1
	1	1	1	
		1	1	
			1	

- **K- MAP FOR Y:**

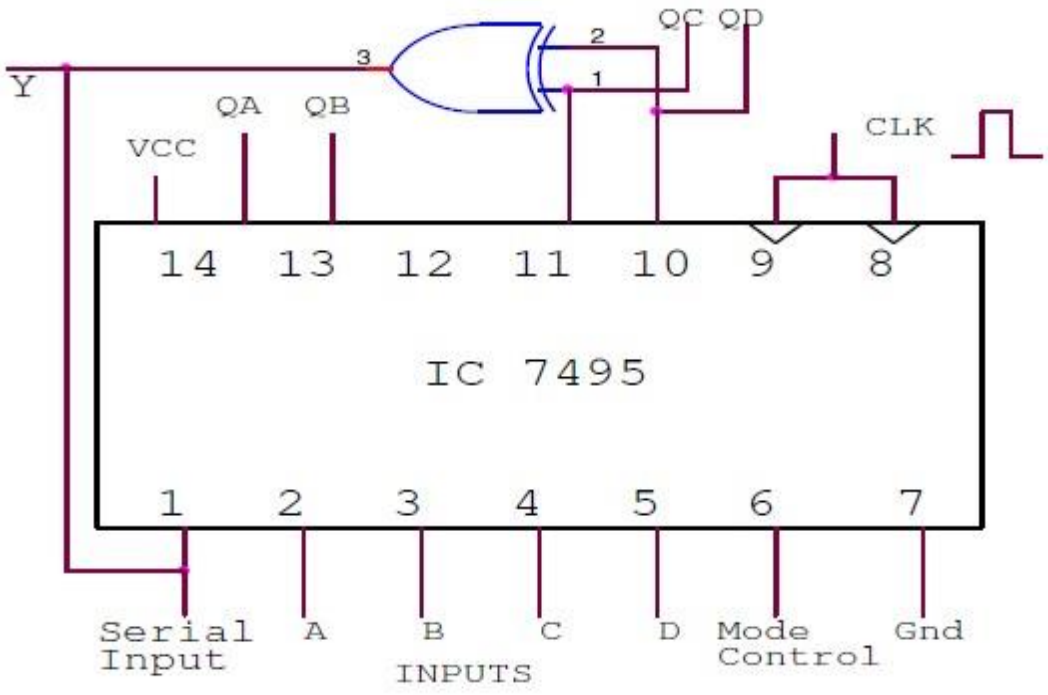
Q3Q2 \ Q1Q0	00	01	11	10
00	X	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

Expression for Y:

$$Y = Q1\overline{Q0} + \overline{Q1}Q0$$

$$Y = Q1 \oplus Q0$$

- **LOGIC DIAGRAM:**



PROCEDURE:

1. Check all the components for their working.
2. Insert the appropriate IC into the IC base.
3. Make connections as shown in the logic diagram.
4. By Keeping mode=1. Load the input A,B,C,D as in Truth Table 1st Row and give a clock pulse
5. For count mode make mode = 0.
6. Verify the Truth Table and observe the outputs.

RESULT: Thus the Sequence generator using shift register is realized & truth tables are verified.

VIVA QUESTIONS:

1. What is the necessity for sequence generation?
2. What are PISO, SIPO, and SISO with respect to shift register? 3.Differentiate between serial data & parallel data

4.What is the significance of Mode control bit?

EXERCISE:

1. Design of the sequence generator for the sequence S = 1001011
2. Design of the sequence generator for the sequence S = 1101011

12.Design Monostable and a stable Multivibrator using 555 Timer.

AIM:Togenerate a pulse using Monostable Multivibrator by using IC555

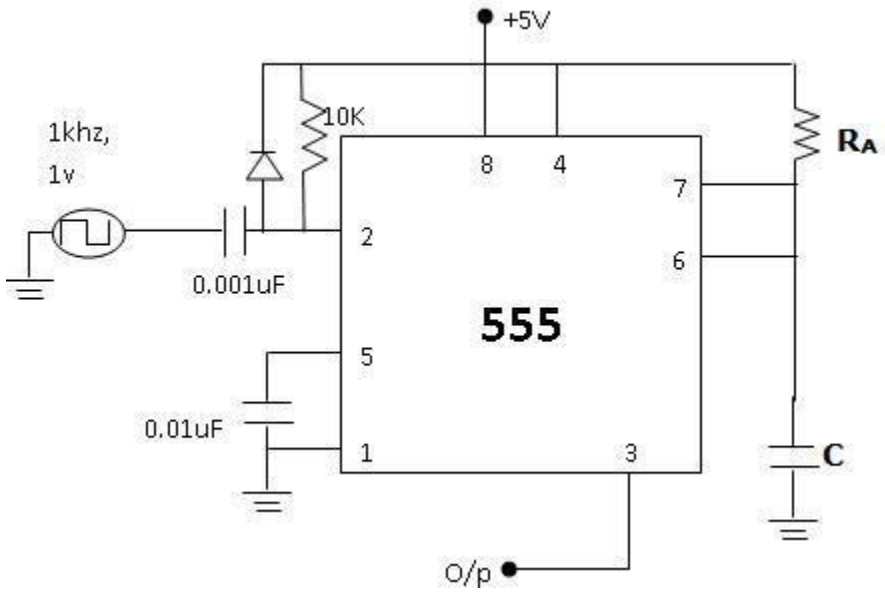
COMPONENTS REQUIRED:

Sl.NO	DESCRIPTION	RANGE	QUANTITY
1	555 IC		1
2	Capacitors	0.1μf,0.01μf	Each one
3	Resistor	10kΩ	1
4	Regulated Power supply	(0 – 30V),1A	1
5	Function Generator	(1HZ – 1MHz)	1
6	Cathode ray oscilloscope	(0 – 20MHz)	1

THEORY:

A Monostable Multivibrator, often called a one-shot Multivibrator, is a pulse-generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby mode the output of the circuit is approximately Zero or at logic-low level. When an external trigger pulse is obtained, the output is forced to go high (V_{CC}). The time for which the output remains high is determined by the external RC network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats. The Monostable circuit has only one stable state (output low), hence the name monostable. Normally the output of the Monostable Multivibrator is low

Monostable Multivibrator Circuit Diagram:

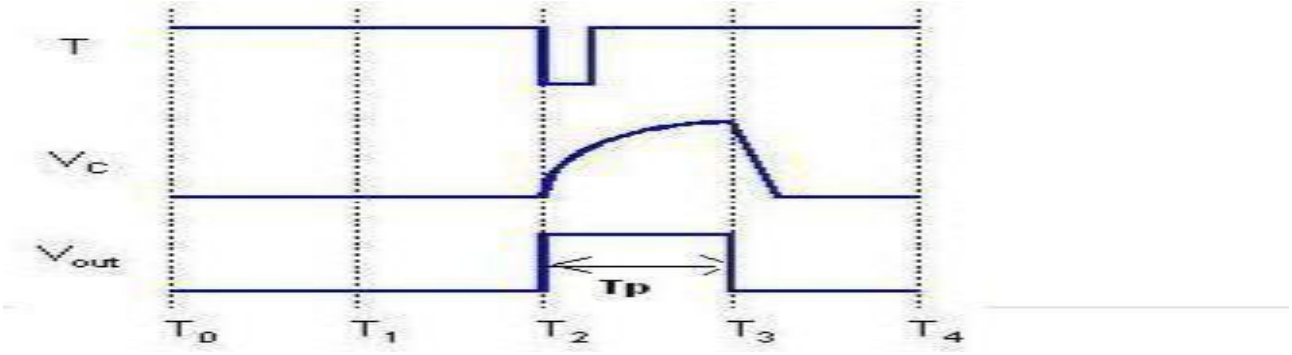


Design: Let the ouput pulse width=T_P =1.1R_AC=1mSec

Choose C=0.1µf,R_A=10KΩ

When triggered by an input pulse, a monostable multivibrator will switch to its unstable position for a period of time, and then return to its stable state. The time period monostable multivibrator remainsinunstablestateisgivenbyt=ln(2)R_2C_1.Ifrepeatedapplicationoftheinputpulsemaintains the circuit in the unstable state, it is called a retriggerable monostable. If further trigger pulses do not affect the period, the circuit is a non-retriggerable multivibrator.

WAVEFORMS:



PROCEDURE:

Monostable Multivibrator

1. Make the connections as shown in fig and switch on the powersupply.
2. Apply 1KHz trigger input to pin 2 of IC 555 through a capacitor0.01µF.
3. Observe the waveform across the timing capacitor(pin 6) and the Pulse output across DC output(pin 3).
4. Verify the designedValues.

Result:

Tp theoretical	Tppractical %
1µs	
2.5 µs	
1ms	
2.2ms	

IC 555 TIMER - ASTABLE OPERATION CIRCUIT

AIM: To generate unsymmetrical square and symmetrical square waveforms usingIC555.

APPARATUS REQUIRED:

Sl.NO	DESCRIPTION	RANGE	QUANTITY
1	IC 555		1
2	Resistors	3.6kΩ,7.2Kω	Each one
3	Capacitors	0.1μf,0.01μf	Each one
4	Diode	OA79	1
5	Regulated Power supply	(0 – 30V),1A	1
6	Cathode Ray Oscilloscope	(0 – 20MHz)	1

THEORY:

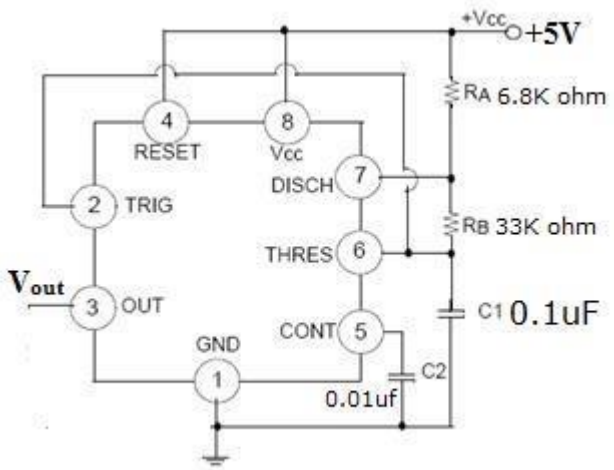
When the power supply V_{CC} is connected, the external timing capacitor 'C" charges oNwards V_{CC} with a time constant (R_A+R_B) C. During this time, pin 3 is high ($\approx V_{CC}$) as Reset R=0,Set S=1 and this combination makes Q =0 which has unclamped the timing capacitor 'C'.When the capacitor voltage equals 2/3 V_{CC}, the upper comparator triggers the control flip flop on that Q =1. It makes Q1 ON and capacitor 'C' starts discharging towards ground through R_B and transistor Q1 with a time constant R_BC. Current also flows into Q1 through R_A. ResistorsR_A and R_B must be large enough to limit this current and prevent damage to the dischargetransistor Q1. The minimum value of R_A is approximately equal to $V_{CC}/0.2$ where 0.2A is the maximum current through the ON transistor Q1.

During the discharge of the timing capacitor C, as it reaches VCC/3, the lower comparator is triggered and at this stage S=1, R=0 which turns Q =0. Now Q =0 unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between 2/3 VCC and 1/3 VCC respectively. The length of time that the output remains HIGH is the time for the capacitor to charge from 1/3 VCC to 2/3 VCC. The capacitor voltage for a low pass RC circuit subjected to a step input of VCC volts is given by VC = VCC [1- exp (-t/RC)]

Total time period T = 0.69 (RA + 2 RB) C

$f= 1/T = 1.44/ (R_A + 2R_B) C$

Circuit Diagram: Astable Multivibrator



Design:

Choose f=1 Khz hence t=1/f=1mSec, Choose dutycycle (D_C) =75%

Duty cycle=$D_c=\frac{T_{on}}{T_{on}+T_{off}}$

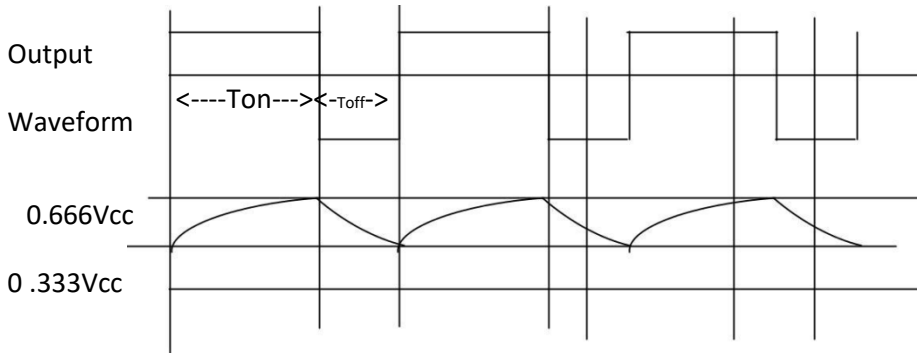
T_{on}=0.75msec, T_{off}=0.25msec

$T_{off}=0.69R_bC$

Choose C=0.1µf,R_b=36KΩ(33 KΩ)

$T_{on}=0.69(R_A+R_B)C$=> R_A=6.8 KΩ

Ideal Waveforms:



PROCEDURE:

Astable Multivibrator

1. Make the connections as shown in fig and switch on the powersupply.
2. Observe the capacitor voltage waveform at 6^{th}pin of 555 timer onCRO.
3. Observe the output waveform at 3^{rd}pin of 555 Timer onCRO.
4. Note down the amplitude levels, time period and hence calculate dutycycle.

Result:

DC theoretical%	Ton theoretical %	Toff theoretical %	Ton practical %	Toff practical %
75				
80				