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SJC INSTITUTE OF TECHNOLOGY

(An Autonomous Institute under VTU, Belagavi)

FIRST SEMESTER M.Tech DEGREE SEMESTER END EXAMINATIONS

MARCH 2026

Course:	**ADVANCED MACHINE LEARNING & DEEP LEARNING**		
Course Code:	**MEC101**	**Program:**	**M.Tech in Digital Communication & Networking**
Max Marks:	**100**	**Duration:**	**03 Hours**

Note:

1. Answer ONE question from each MODULE and Question 1 & 2 is compulsory.
2. Any missing Data can be suitably assumed.

Q.No.		**MODULE - 1**	**Marks**	**CO**	**RBTL**
Q1	**a**	Explain classification and regression in the context of supervised learning	**4**	**1**	**L2**
	b	Build a k-neighbors regression model using scikit-learn and analyze the effect of different values of n_neighbors on the results	**8**	**3,4**	**L3**
	c	Develop a linear support vector machine (SVM) classifier using scikit-learn and test it on a multiclass dataset.	**8**	**2**	**L3**
		MODULE – 2			
Q2	**a**	Explain the main challenges associated with unsupervised learning and how they differ from supervised learning	**4**	**1**	**L1**
	b	Make use of Principal Component Analysis (PCA) on a dataset and demonstrate how the number of components affects data reconstruction.	**8**	**1**	**L3**
	c	Apply Non-Negative Matrix Factorization (NMF) to decompose a dataset and analyze its application in topic modeling.	**8**	**3,4**	**L3**
		MODULE – 3			
Q3	**a**	Explain the Convolution Operation along with an example of 2-D convolution without kernel-flipping.	**6**	**1**	**L1**
	b	Build pooling function to modify the output of the layer at third stage of convolution network.	**8**	**1**	**L3**
	c	Apply Structured Outputs with the effect of zero padding on network size.	**6**	**2**	**L3**
		OR			
Q4	**a**	Illustrate Variants of the Basic Convolution Function.	**6**	**1**	**L2**
	b	Interpret how the Neuro scientific basis for Convolutional Networks.	**8**	**1**	**L2**
	c	Organize Random or Unsupervised features along with three basic strategies.	**6**	**4**	**L3**

MODULE – 4					
Q5	**a**	Summarize Recurrent Neural Networks with examples.	**6**	**1**	**L1**
	b	Construct Encoder-Decoder Sequence-to-Sequence Architectures.	**6**	**1**	**L3**
	c	Model the Recursive Neural Networks.	**8**	**3**	**L3**
OR					
Q6	**a**	Explain Deep Recurrent Networks.	**6**	**1**	**L1**
	b	Infer the Long Short-Term Memory and Other Gated RNNs.	**8**	**1**	**L2**
	c	Build Optimization for Long-Term Dependencies.	**6**	**3**	**L3**
MODULE – 5					
Q7	**a**	Explain Model Compression.	**6**	**1**	**L1**
	b	Analyze speech recognition to map acoustic signal containing a spoken natural language utterance into the corresponding sequence	**8**	**2,3**	**L3**
	c	Apply Large-Scale Deep Learning for accuracy and the improvement of the complexity.	**6**	**4**	**L4**
OR					
Q8	**a**	Explain Neural Machine Translation	**6**	**1**	**L1**
	b	Construct Computer Vision along with its preprocessing.	**6**	**2,3**	**L3**
	c	Examine various applications of deep learning.	**8**	**4**	**L4**

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FIRST SEMESTER M.Tech DEGREE SEMESTER END EXAMINATIONS

MARCH 2026

Course:	**ADVANCED EMBEDDED SYSTEM**		
Course Code:	**MEC102**	**Program:**	**M.Tech in Digital Communication & Networking**
Max Marks:	**100**	**Duration:**	**03 Hours**

Note:

1. Answer ONE question from each MODULE and Question 1 & 2 is compulsory.
2. Any missing Data can be suitably assumed.

Q.No.		**MODULE - 1**	**Marks**	**CO**	**RBTL**
Q1	**a**	What is embedded system? Outline the elements of an embedded system	**6**	**1**	**L1**
	b	Compare Vonneumann and Harvard architecture	**6**	**1**	**L2**
	c	Analyze the key functionalities of the I^{2}C protocol in embedded systems.	**8**	**1**	**L3**
		MODULE – 2			
Q2	**a**	Distinguish data flow graph (DFG) and control Data Flow Graph(CDFG)mode?	**6**	**1**	**L1**
	b	Discuss the various operational quality attributes of an embedded systems in detail.	**6**	**1**	**L2**
	c	Develop the FSM model of an automatic vending machine that can dispense tea or coffee	**8**	**1**	**L3**
		MODULE – 3			
Q3	**a**	Define ARM Thumb2 Technology .	**6**	**2**	**L1**
	b	Write a note on special registers and their functions in ARM cortex M3.	**6**	**2**	**L2**
	c	Analyze the architecture of ARM Cortex-M3 and identify how the various functional units interact during program execution.	**8**	**2**	**L3**
		OR			
Q4	**a**	List and explain the ARM Cortex-M3 processor registers.	**6**	**2**	**L1**
	b	Outline any six applications of ARM with an example.	**6**	**2**	**L2**
	c	Analyze the internal working of the stack during PUSH and POP operations in ARM Cortex-M3.	**8**	**2**	**L3**

MODULE – 4					
Q5	**a**	Write a note on Interrupts (NVIC), built in ARM Cortex-M3.	**4**	**2**	**L1**
	b	Write simple ARM assembly code examples to show how each of the following instructions works i) LSLW ii) RORW iii) STRH iv) MRS,	**8**	**2**	**L3**
	c	Develop ARM Cortex-M assembly language program to compute the sum of the first 10 natural numbers (sum = 1 + 2 + ... + 10)	**8**	**4**	**L4**
OR					
Q6	**a**	Explain the SystemTick timer.	**4**	**2**	**L1**
	b	Write simple ARM assembly code examples to show how each of the following instructions works i) CMN ii)EOR iii) MOV iv) SVC	**8**	**2**	**L2**
	c	Develop C language program to switch ON or OFF an LED with required delay	**8**	**4**	**L4**
MODULE – 5					
Q7	**a**	Define a process and list the main components of its structure.	**4**	**3**	**L1**
	b	What is RTOS? describe the services provided by a real-time kernel.	**8**	**3**	**L2**
	c	Three processes with process IDs P1,P2,P3 with the estimated completion time 6,4,2 milli seconds respectively enters the ready queue together in the order P1,P2,P3.Calculate the waiting time and turn around time for each process and the average waiting time and turn around time in RR algorithm with time slice=2ms.	**8**	**3**	**L3**
OR					
Q8	**a**	Define Preemptive and Non-Preemptive Scheduling algorithm	**4**	**3**	**L1**
	b	What is Deadlock? Outline conditions favoring a deadlock situation.	**8**	**3**	**L2**
	c	Three processes with process IDs P1,P2,P3 with the estimated completion time 10,5,7 milli seconds respectively enters the ready queue together. A new process P4 with estimated completion time 2 ms enters the 'Ready' queue after 2ms of execution of P2. Calculate the waiting time and turn around time for each process and the average waiting time and turn around time in preemptive SJF scheduling.	**8**	**3**	**L3**

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FIRST SEMESTER M.Tech DEGREE SEMESTER END EXAMINATIONS

MARCH 2026

Course:	**DIGITAL CIRCUITS & LOGIC DESIGN**		
Course Code:	**MEC103**	**Program:**	**M.Tech in Digital Communication & Networking**
Max Marks:	**100**	**Duration:**	**03 Hours**

Note:

1. Answer ONE question from each MODULE and Question 1 & 2 is compulsory.
2. Any missing Data can be suitably assumed.

<table>
<tr><th colspan="2">Q.No.</th><th>MODULE - 1</th><th>Marks</th><th>CO</th><th>RBTL</th></tr>
<tr><td rowspan="3">Q1</td><td>a</td><td>Define the concept of a finite-state model.</td><td>4</td><td>1</td><td>L1</td></tr>
<tr><td>b</td><td>Explain the concept of threshold logic and outline the various capabilities of threshold element.</td><td>8</td><td>1</td><td>L2</td></tr>
<tr><td>c</td><td>Solve the given function f $(x_1, x_2, x_3, x_4) =\Sigma (0,1,2,3,7,11)$ is a threshold function if yes, find the weight-threshold vectors.</td><td>8</td><td>1</td><td>L3</td></tr>
<tr><td colspan="6">MODULE – 2</td></tr>
<tr><td rowspan="3">Q2</td><td>a</td><td>Define the static hazard with an example</td><td>4</td><td>2</td><td>L1</td></tr>
<tr><td>b</td><td>For the given function f(a,b,c,d)=a'b'+b'c'+abcd, find the a-test and b-test values.</td><td>8</td><td>2</td><td>L2</td></tr>
<tr><td>c</td><td>Explain and analyze the Detection of multiple faults in the Digital circuit.</td><td>8</td><td>2</td><td>L3</td></tr>
<tr><td colspan="6">MODULE – 3</td></tr>
<tr><td rowspan="3">Q3</td><td>a</td><td>Explain the Boolean differences with an example.</td><td>4</td><td>3</td><td>L2</td></tr>
<tr><td>b</td><td>For the incompletely specified machine shown in Table.Q3(b), Calculate a minimum-state reduced machine containing the original one.
<table>
<tr><th rowspan="2">PS</th><th colspan="3">NS, Z</th></tr>
<tr><th>I_1</th><th>I_2</th><th>I_3</th></tr>
<tr><td>A</td><td>C,0</td><td>E,1</td><td>--</td></tr>
<tr><td>B</td><td>C,0</td><td>E,1</td><td>--</td></tr>
<tr><td>C</td><td>B, -</td><td>C,0</td><td>A, -</td></tr>
<tr><td>D</td><td>B,0</td><td>C, -</td><td>E, -</td></tr>
<tr><td>E</td><td>--</td><td>E,0</td><td>A,-</td></tr>
</table></td><td>8</td><td>3</td><td>L3</td></tr>
<tr><td>c</td><td>Analyze the fault location experiments and explain the properties of Boolean difference.</td><td>8</td><td>3</td><td>L3</td></tr>
<tr><td colspan="6">OR</td></tr>
</table>

<table>
<tr><td rowspan="3">Q4</td><td>a</td><td>Outline the merger graph in detail with a suitable example</td><td>4</td><td>3</td><td>L2</td></tr>
<tr><td>b</td><td>Given the fault shown in the table, where Z denotes the fault-free output for the corresponding test
(i) Calculate a minimal set of tests to detect single faults
(ii) Find a preset set of tests to locate all single faults and show the corresponding fault dictionary
(iii) Determine a minimal adaptive fault -location experiment
<table>
<tr><th>Test/fault</th><th>F1</th><th>F2</th><th>F3</th><th>F4</th><th>F5</th><th>Z</th></tr>
<tr><td>T1</td><td></td><td></td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>T2</td><td>1</td><td>1</td><td></td><td></td><td></td><td>1</td></tr>
<tr><td>T3</td><td></td><td></td><td></td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>T4</td><td></td><td>1</td><td></td><td></td><td></td><td>0</td></tr>
<tr><td>T5</td><td></td><td></td><td></td><td></td><td>1</td><td>1</td></tr>
</table>
</td><td>8</td><td>3</td><td>L3</td></tr>
<tr><td>c</td><td>Analyze the Adaptive fault location experiments with an example.</td><td>8</td><td>3</td><td>L3</td></tr>
<tr><td colspan="6">MODULE – 4</td></tr>
<tr><td rowspan="3">Q5</td><td>a</td><td>Interpret the Input-consistent and Output-consistent with respect to sequential machines</td><td>4</td><td>4</td><td>L2</td></tr>
<tr><td>b</td><td>For the machine M1 in Table.Q5(b), find the equivalence partition and a corresponding reduced machine in the standard form. Determine a minimum length sequence that distinguishes state A from state B.
<table>
<tr><th rowspan="2">PS</th><th colspan="2">NS, Z</th></tr>
<tr><th>X=0</th><th>X=1</th></tr>
<tr><td>A</td><td>B,1</td><td>H,1</td></tr>
<tr><td>B</td><td>F,1</td><td>D,1</td></tr>
<tr><td>C</td><td>D,0</td><td>E,1</td></tr>
<tr><td>D</td><td>C,0</td><td>F,1</td></tr>
<tr><td>E</td><td>D,1</td><td>C,1</td></tr>
<tr><td>F</td><td>C,1</td><td>C,1</td></tr>
<tr><td>G</td><td>C,1</td><td>D,1</td></tr>
<tr><td>H</td><td>C,0</td><td>A,1</td></tr>
</table>
</td><td>8</td><td>4</td><td>L3</td></tr>
<tr><td>c</td><td>Describe the Closed partition, Lattice, implication graph and partition pair of the sequential machines.</td><td>8</td><td>4</td><td>L3</td></tr>
<tr><td colspan="6">OR</td></tr>
<tr><td rowspan="2">Q6</td><td>a</td><td>Explain with an example, how the state assignment can reduce the structure of a sequential machine.</td><td>4</td><td>4</td><td>L2</td></tr>
<tr><td>b</td><td>DeDerive the following theorems:
i) The equivalence partition is unique.
ii) If two states S_i and S_j of machine 'M' are distinguishable, then they are distinguishable by a sequence of length n - 1 or less, where n is the number of states in 'M'</td><td>8</td><td>4</td><td>L3</td></tr>
</table>

<table>
<tr><td></td><td>c</td><td>Solve the Π - lattice of the machine shown in Table -6c below.
<table>
<tr><th rowspan="2">PS</th><th colspan="2">NS</th><th>Z</th></tr>
<tr><th>X=0</th><th>X=1</th><th></th></tr>
<tr><td>A</td><td>H</td><td>B</td><td>0</td></tr>
<tr><td>B</td><td>F</td><td>A</td><td>0</td></tr>
<tr><td>C</td><td>G</td><td>D</td><td>0</td></tr>
<tr><td>D</td><td>E</td><td>C</td><td>1</td></tr>
<tr><td>E</td><td>A</td><td>C</td><td>0</td></tr>
<tr><td>F</td><td>C</td><td>D</td><td>0</td></tr>
<tr><td>G</td><td>B</td><td>A</td><td>0</td></tr>
<tr><td>H</td><td>D</td><td>B</td><td>0</td></tr>
</table></td><td>8</td><td>4</td><td>L3</td></tr>
<tr><td colspan="6">MODULE – 5</td></tr>
<tr><td rowspan="3">Q7</td><td>a</td><td>Outline the compatible states in the sequential machines.</td><td>4</td><td>5</td><td>L2</td></tr>
<tr><td>b</td><td>What are definitively diagnosable machines? Check whether a distinguishable sequence exists for the machine shown in Table – 7b. Analyze the testing graph for the same.
<table>
<tr><th rowspan="2">PS</th><th colspan="2">NS, Z</th></tr>
<tr><th>X=0</th><th>X=1</th></tr>
<tr><td>A</td><td>B,0</td><td>C,1</td></tr>
<tr><td>B</td><td>C,0</td><td>D,0</td></tr>
<tr><td>C</td><td>D,1</td><td>C,1</td></tr>
<tr><td>D</td><td>A,1</td><td>B,0</td></tr>
</table></td><td>8</td><td>5</td><td>L3</td></tr>
<tr><td>c</td><td>Explain the synchronizing experiments analyze with an example in the sequential machines</td><td>8</td><td>5</td><td>L3</td></tr>
<tr><td colspan="6">OR</td></tr>
<tr><td rowspan="3">Q8</td><td>a</td><td>Infer the Homing experiments in the sequential machines</td><td>4</td><td>5</td><td>L1</td></tr>
<tr><td>b</td><td>Explain the diagnosable sequence machine and construct the testing table and graph for machine shown in Table Q.8(b)
<table>
<tr><th rowspan="2">PS</th><th colspan="2">NS, Z</th></tr>
<tr><th>X=0</th><th>X=1</th></tr>
<tr><td>A</td><td>B,0</td><td>D,0</td></tr>
<tr><td>B</td><td>A,0</td><td>B,0</td></tr>
<tr><td>C</td><td>D,1</td><td>A,0</td></tr>
<tr><td>D</td><td>D,1</td><td>C,0</td></tr>
</table></td><td>8</td><td>5</td><td>L3</td></tr>
<tr><td>c</td><td>Make use of the general procedure for the fault detection experiment for the machine that has a distinguishable sequence with repeated symbols.</td><td>8</td><td>5</td><td>L3</td></tr>
</table>

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FIRST SEMESTER M.Tech DEGREE SEMESTER END EXAMINATIONS

MARCH 2026

Course:	**ADVANCED SIGNAL PROCESSING**		
Course Code:	**MEC114C**	**Program:**	**M.Tech in Digital Communication & Networking**
Max Marks:	**100**	**Duration:**	**03 Hours**

Note:

1. Answer ONE question from each MODULE and Question 1 & 2 is compulsory.
2. Any missing Data can be suitably assumed.

Q.No.		**MODULE - 1**	**Marks**	**CO**	**RBTL**
Q1	**a**	Explain the Digital Signal Processing system with necessary block Diagram	**6**	**1**	**L1**
	b	Determine IDFT using DFT and then find IDFT of 4-point sequence X(k)=[4,-2j,0,2j] using DFT	**8**	**1**	**L2**
	c	Solve for Inverse *z*-Transform using Partial Fraction Method $x(z) = \frac{1}{1-1.5z^{-1}+0.5z^{-2}}$ $with\ ROC\ \lvert z\rvert > 1$	**6**	**1**	**L3**
		MODULE – 2			
Q2	**a**	Mention 4 Difference between IIR and FIR Filter.	**4**	**2**	**L1**
	b	Design an FIR filter to approx. an an ideal LPF with passband Gain of unity cutoff frequency of 850HZ & working at sampling frequency of 5000HZ the length of impulse response should be 5. Use Hamming Window .	**10**	**2**	**L3**
	c	Design a second order digital Butterworth filter with cutoff frequency of 1kHZ and sampling frequency of 10^4 samples/sec by using bilinear transformation .	**6**	**2**	**L5**
		MODULE – 3			
Q3	**a**	Define Decimation technique with the help of neat block diagram.	**6**	**3**	**L1**
	b	With Suitable mathematical expression illustrate the working of adaptive noise cancelling systems.	**8**	**3**	**L2**
	c	Apply Sampling rate conversion technology in the working of CD Audio player using Neat Block Diagram	**6**	**3**	**L3**
		OR			
Q4	**a**	Show the effect of aliasing and spectrum of a down sampler with necessary waveforms.	**6**	**3**	**L1**
	b	Derive the expression for the spectrum of an up sampler with necessary equations.	**8**	**3**	**L2**

	c	Utilize the sinusoidal sequence to derive and explain the decimation process.	**6**	**3**	**L3**
		MODULE – 4			
Q5	**a**	Mention the applications of Analysis and Synthesis Filter Banks.	**6**	**4**	**L1**
	b	Illustrate the adapter filtering method in Linear Predictive Coding (LPC) to encode speech signal.	**8**	**4**	**L2**
	c	Utilize the concept of two channel quadrature mirror filter bank to derive necessary equations in matrix for the two filter.	**6**	**4**	**L3**
		OR			
Q6	**a**	Define Polyphase Filter Structure and Implementation	**6**	**4**	**L1**
	b	Illustrate Working of Poly Phase Filters in Multirate Signal Processing using a neat block diagram.	**8**	**4**	**L2**
	c	Given the polyphase matrix for a three channel perfect reconstruction FIR QMF bank is P(Z^3)=[1 1 2 ; 2 3 1;1 2 1] . Solve for the analysis and synthesis filters in the QMF Bank.	**6**	**4**	**L3**
		MODULE – 5			
Q7	**a**	With neat sketch Define i) 2D Impulse Function ii) 2D Step Function.	**4**	**5**	**L1**
	b	Outline the steps involved in DCT based signal Compression. Show the necessary mathematical expressions.	**6**	**5**	**L2**
	c	Evaluate Covariance matrix, Eigen Values and Eigen Vectors, Kernel for x=[4 -2 ; -1 3] by utilizing mathematical foundation of the KLT	**10**	**5**	**L4**
		OR			
Q8	**a**	Define Linearity and Separable Properties of 2 D DFT .	**4**	**5**	**L1**
	b	Explain Compression concept using DCT and Determine the 2D - DCT coefficients for the following image: [100 50 ; 100 10]	**6**	**5**	**L2**
	c	Prove that the 2D DFT is both linear and separable. Then, given an N×N image matrix, explain how Separability can be leveraged to reduce computational complexity when implementing the 2D DFT efficiently using a series of 1D DFTs.	**10**	**5**	**L4**

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FIRST SEMESTER M.Tech DEGREE SEMESTER END EXAMINATIONS

MARCH 2026

Course:	**MULTIMEDIA AND APPLICATIONS**		
Course Code:	**MEC115C**	**Program:**	**M.Tech in Digital Communication & Networking**
Max Marks:	**100**	**Duration:**	**03 Hours**

Note:

1. Answer ONE question from each MODULE and Question 1 & 2 is compulsory.
2. Any missing Data can be suitably assumed.

Q.No.		**MODULE - 1**	**Marks**	**CO**	**RBTL**
Q1	**a**	List and outline the different types of Multimedia networks used to provide Multimedia communication services.	**6**	**1**	**L1**
	b	Explain network QoS associated with circuit switched networks.	**8**	**2**	**L2**
	c	Design and explain the signal encoder & decoder. Also draw the associated waveforms.	**6**	**1**	**L3**
		MODULE – 2			
Q2	**a**	What are the merits and demerits of digitization of audio signal?	**4**	**1**	**L1**
	b	Illustrate the concept of run-length coding and statistical encoding with an example.	**10**	**3**	**L2**
	c	A series of messages is to be transferred between two computers over a PSTN. The messages comprise just the characters A through H. Analysis has shown that the probability of occurrence of each character is as follows: A and B=0.25, C and D=0.14, E, F, G and H=0.055 Derive the average number of bits per character for your codeword set and compare this with: i) The entropy of the messages (Shannon's value) ii) Fixed-length binary codewords. iii) 7-bit ASCII codewords.	**6**	**3**	**L3**
		MODULE – 3			
Q3	**a**	Define DPCM and Explain the operation of a basic DPCM signal encoder with the help of block diagram.	**6**	**3**	**L2**
	b	Explain MPEG perceptual encoder/decoder implementation schematic and give an example frame format.	**7**	**3**	**L2**
	c	Illustrate with a neat diagram, Dolby AC-2, Apply hybrid backward / forward adaptive bit allocation to overcome the disadvantages of Dolby AC-2-bit allocation.	**7**	**3**	**L3**

OR

Q4	**a**	What is ADPCM? Discuss about ADPCM the sub-band Decoder with a schematic.	**6**	**3**	**L1**
	b	Explain the principles on which LPC codes are based, hence with the aid of a schematic diagram of an LPC encoder and decoder.	**7**	**3**	**L2**
	c	Make use of perceptual coding to explain the sensitivity of the earing frequency and temporal masking with relevant diagrams.	**7**	**3**	**L3**

MODULE – 4

Q5	**a**	Define GOP, Prediction span, motion estimation and compensation?	**6**	**4**	**L1**
	b	Explain with neat diagram of video compression principle.	**8**	**4**	**L2**
	c	Apply the concept of Reversible VLCs to explain the effect of transmission errors on decoding procedure.	**6**	**4**	**L3**

OR

Q6	**a**	What is H.263? Discuss Error resilience in H.263 standard.	**6**	**4**	**L1**
	b	Outline H.261 video compression standard with the help of macro block format, frame format and GOB structure.	**8**	**4**	**L2**
	c	A digitized video is to be compressed using the MPEG-1 standard. Assuming a frame sequence of: IBBPBBPBBPBBI….. and average compression ratios of 10:1 (I), 20:1 (P) and 50:1 (B), derive the average bit rate that is generated by the encoder for PAL digitization format.	**6**	**4**	**L3**

MODULE – 5

Q7	**a**	Define the term Quality of Service (QoS). Infer the qualities of traffic.	**6**	**2**	**L1**
	b	Describe transport of MPEG-4 across ATM network with a suitable diagram.	**8**	**2**	**L2**
	c	Analyze packet audio in the network environment.	**6**	**1**	**L4**

OR

Q8	**a**	What is RTP? Discuss the features of RTP.	**6**	**2**	**L1**
	b	Explain in detail about the circuit switching with a neat diagram.	**8**	**2**	**L2**
	c	Analyze packet video in the network environment.	**6**	**1**	**L4**