

MICROCONTROLLER AND EMBEDDED SYSTEMS
(Effective from the academic year 2018 -2019)

SEMESTER – IV

Course Code	18CS44	CIE Marks	40
Number of Contact Hours/Week	3:0:0	SEE Marks	60
Total Number of Contact Hours	40	Exam Hours	03

CREDITS –3

Course Learning Objectives: This course (18CS44) will enable students to:

- Understand the fundamentals of ARM based systems, basic hardware components, selection methods and attributes of an embedded system.
- Program ARM controller using the various instructions
- Identify the applicability of the embedded system
- Comprehend the real time operating system used for the embedded system

Module 1	Contact Hours
<p>Microprocessors versus Microcontrollers, ARM Embedded Systems: The RISC design philosophy, The ARM Design Philosophy, Embedded System Hardware, Embedded System Software. ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts, and the Vector Table , Core Extensions Text book 1: Chapter 1 - 1.1 to 1.4, Chapter 2 - 2.1 to 2.5 RBT: L1, L2</p>	08
<p>Module 2 Introduction to the ARM Instruction Set : Data Processing Instructions , Programme Instructions, Software Interrupt Instructions, Program Status Register Instructions, Coprocessor Instructions, Loading Constants ARM programming using Assembly language: Writing Assembly code, Profiling and cycle counting, instruction scheduling, Register Allocation, Conditional Execution, Looping Constructs Text book 1: Chapter 3:Sections 3.1 to 3.6 (Excluding 3.5.2), Chapter 6(Sections 6.1 to 6.6) RBT: L1, L2</p>	08
<p>Module 3 Embedded System Components: Embedded Vs General computing system, History of embedded systems, Classification of Embedded systems, Major applications areas of embedded systems, purpose of embedded systems Core of an Embedded System including all types of processor/controller, Memory, Sensors, Actuators, LED, 7 segment LED display, stepper motor, Keyboard, Push button switch, Communication Interface (onboard and external types), Embedded firmware, Other system components. Text book 2:Chapter 1(Sections 1.2 to 1.6),Chapter 2(Sections 2.1 to 2.6) RBT: L1, L2</p>	08
<p>Module 4 Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational quality attributes ,non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modelling, embedded firmware design and development Text book 2: Chapter-3, Chapter-4, Chapter-7 (Sections 7.1, 7.2 only), Chapter-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only) RBT: L1, L2</p>	08

Module 5	
<p>RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Multiprocessing and Multitasking, Task Communication (without any program), Task synchronization issues – Racing and Deadlock, Concept of Binary and counting semaphores (Mutex example without any program), How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil), Disassembler/decompiler, simulator, emulator and debugging techniques, target hardware debugging, boundary scan.</p> <p>Text book 2: Chapter-10 (Sections 10.1, 10.2, 10.3, 10.4 , 10.7, 10.8.1.1, 10.8.1.2, 10.8.2.2, 10.10 only), Chapter 12, Chapter-13 (block diagram before 13.1, 13.3, 13.4, 13.5, 13.6 only)</p> <p>RBT: L1, L2</p>	08
<p>Course Outcomes: The student will be able to :</p>	
<ul style="list-style-type: none"> • Describe the architectural features and instructions of ARM microcontroller • Apply the knowledge gained for Programming ARM for different applications. • Interface external devices and I/O with ARM microcontroller. • Interpret the basic hardware components and their selection method based on the characteristics and attributes of an embedded system. • Develop the hardware /software co-design and firmware design approaches. • Demonstrate the need of real time operating system for embedded system applications 	
<p>Question Paper Pattern:</p>	
<ul style="list-style-type: none"> • The question paper will have ten questions. • Each full Question consisting of 20 marks • There will be 2 full questions (with a maximum of four sub questions) from each module. • Each full question will have sub questions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module. 	
<p>Textbooks:</p>	
<ol style="list-style-type: none"> 1. Andrew N Sloss, Dominic Symes and Chris Wright, ARM system developers guide, Elsevier, Morgan Kaufman publishers, 2008. 2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education, Private Limited, 2nd Edition. 	
<p>Reference Books:</p>	
<ol style="list-style-type: none"> 1. Raghunandan..G.H, Microcontroller (ARM) and Embedded System, Cengage learning Publication,2019 2. The Insider's Guide to the ARM7 Based Microcontrollers, Hitex Ltd.,1st edition, 2005. 3. Steve Furber, ARM System-on-Chip Architecture, Second Edition, Pearson, 2015. 4. Raj Kamal, Embedded System, Tata McGraw-Hill Publishers, 2nd Edition, 2008. 	

DELIVERY PLAN WITH DETAILS

MODULE – 1

Lecture #	Topic	Mode of Delivery (Pls Tick ✓)				Date of Delivery	COs Covered
		1	2	3	4		
1	Microprocessors versus Microcontrollers			✓		19/4/21	CO1
2	ARM Embedded Systems: The RISC design philosophy			✓		20/4/21	CO1
3	The ARM Design Philosophy			✓		27/4/21	CO1
4	Embedded System Hardware			✓		28/4/21	CO1
5	Embedded System Software			✓		30/4/21	CO1
6	ARM Processor Registers			✓		4/5/21	CO1
7	Current Program Status Register, Pipeline			✓		4/5/21	CO1
8	Exceptions, Interrupts			✓		7/5/21	CO1
9	The Vector Table, Core Extensions			✓		11/5/21	CO1
10	Revision of important topics EDMODO test on module contents			✓		18/5/21	CO1

Textbook : and chapter : TBI, Chapter 1, Chapter 2

Signatures	Faculty:	#HOURS	Allotted	Taken
	HOD:		10	10
Remarks				

MODULE – 2

Lecture #	Topic	Mode of Delivery (Pls Tick ✓)				Date of Delivery	COs Covered
		1	2	3	4		
1	Introduction to the ARM Instruction Set			✓		12/5/21	CO2
2	Data Processing Instructions			✓		19/5/21	CO2
3	S/w Interrupt Instructions,			✓		19/5/21	CO2
4	Program Status Register Instructions			✓		20/5/21	CO2
5	Coprocessor Instructions, Loading Constants			✓		21/5/21	CO2
6	ARM prog using Assembly language: Writing Assembly code			✓		25/5/21	CO2
7	Profiling and cycle counting,			✓		26/5/21	CO2
8	instruction scheduling , Register Allocation,			✓		26/5/21	CO2
9	Conditional Execution, Looping Constructs			✓		1/6/21	CO2
10	Presentation on topics of the module., EDMODO test on module contents			✓			CO6

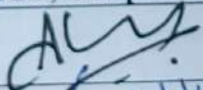
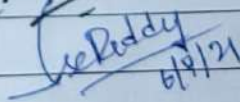
Textbook : and chapter: TBI, Chapter 3, Chapter 6

Signatures	Faculty:	#HOURS	Allotted	Taken
	HOD:		10	09

MODULE - 3

Lecture #	Topic	Mode of Delivery (Pls Tick ✓)				Date of Delivery	COs Covered
		1	2	3	4		
1	Embedded System Components: Embedded Vs General computing system, History of embedded systems			✓		4/6/21	CO3
2	Types of Embedded systems, Major applications of ES			✓		7/6/21	CO3
3	Purpose of embedded systems			✓		8/6/21	CO3
4	Core of an Embedded System			✓		9/6/21	CO3
5	Memory, Sensors, Actuators			✓		11/6/21	CO3
6	LED, 7 segment LED display,			✓		15/6/21	CO3
7	stepper motor			✓		15/6/21	CO3
8	Keyboard, Push button switch, Communication Interface			✓		22/6/21	CO3
9	Embedded firmware, Other system components.			✓		22/6/21	CO3
10	Presentation on topics of the module.			✓		22/6/21	CO6

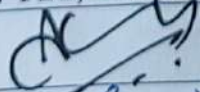
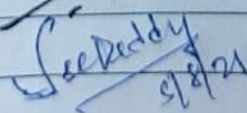
Textbook : and chapter : TB2, Chapter 1, Chapter 2

Signatures	Faculty: 	#HOURS	Allotted	Taken
	HOD: 		10	10
Remarks				

MODULE - 4

Lecture #	Topic	Mode of Delivery (Pls Tick ✓)				Date of Delivery	COs Covered
		1	2	3	4		
1	Embedded System Design Concepts:			✓		23/6/21	CO4
2	Characteristics and Quality Attributes of Embedded Systems			✓		23/6/21	CO4
3	Operational quality attributes			✓		25/6/21	CO4
4	& non-operational quality attributes			✓		25/6/21	CO4
5	Embedded Systems-Application			✓		2/7/21	CO4
6	Domain specific applications			✓		2/7/21	CO4
7	Hardware Software Co-Design			✓		6/7/21	CO4
8	Program Modeling			✓		7/7/21	CO4
9	Embedded firmware design and development			✓		7/7/21	CO4
10	Presentation on topics of the module.			✓			CO6

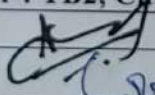
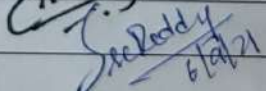
Textbook: and chapter : TB2, Chapter 3, Chapter 4, Chapter 7, Chapter 9

Signatures	Faculty: 	#HOURS	Allotted	Taken
	HOD: 		10	10
Remarks				

MODULE - 5

Lecture #	Topic	Mode of Delivery (Pls Tick ✓)				Date of Delivery	COs Covered
		1	2	3	4		
1	Operating System basics, Types of operating systems Task, process and threads			✓		2/7/21	CO5
2	Thread preemption Multiprocessing and Multitasking, Task Communication			✓		2/7/21	CO5
3	Task synchronization issues – Racing and Deadlock			✓		9/7/21	CO5
4	Concept of Binary and counting semaphores, How to choose an RTOS			✓		13/7/21	CO5
5	Integration and testing of Embedded hardware and firmware			✓		14/7/21	CO5
6	Embedded system Development Environment – Block diagram			✓		20/7/21	CO5
7	Disassembler /decompiler, simulator, emulator and debugging techniques,			✓		23/7/21	CO5
8	target hardware debugging, boundary scan			✓		27/7/21	CO5
9	Presentation on topics of the module.			✓		28/7/21	CO5
10	Demonstrate an unique real time application of ARM controller			✓		29/7/21	CO5

Textbook : and chapter : TB2, Chapter 10, Chapter 12, Chapter 13

Signatures	Faculty: 	#HOURS	Allotted	Taken
	HOD: 		10	10
Remarks				

Text Books:

1. ARM system developers guide, Andrew N Sloss, Dominic Symes and Chris Wright, Elsevier, Morgan Kaufman publishers, 5TH Edition, 2008
2. "Introduction to Embedded Systems", Shibu K V, Tata McGraw Hill, 2nd edition, 2008

Reference Books:

1. Microcontroller (ARM) and Embedded System, Raghunandan..G.H
2. The Insider's Guide to the ARM7 Based Microcontrollers
3. ARM System-on-Chip Architecture, Steve Furber

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Summary of Course Outcomes

Weight, %	Attainment				Blooms Levels	
	40	50	10		Level's	No.
CO-Number	CIE	SEE	CES	Total		
C214.1	3	1.5	3	2.3		
C214.2	3	1.5	3	2.3		
C214.3	3	1.5	3	2.3		
C214.4	3	1.5	3	2.3		
C214.5	3	1.5	3	2.3		
C214.6	3	1.5	3	2.3		

E. Students Feedback

Over all feedback value

F. Remarks on CIE, attainment and suggestion(s) to improve course delivery by course instructor

All COs & POs targets are achieved.

G. Innovative/Best methods used for course delivery by the course instructor

Used more practical demonstration & Presentations of important topics by students

H. Remarks of the Module Coordinator

Com inson the CO & PO targets

Signature
Name

Module Coordinator

Signature of the HOD

Abdul Khadar A/Sabin T T
Course Instructor

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A. Course Details

Course Title	MICROPROCESSORS AND EMBEDDED SYSTEMS				Course Code	C214	
Subject Code	18CS44	Semester	4	Section	A & B	Programme	UG
Course		Course Type			No. of students	119	
Date of commencement				Date of Closure			

B. Course Instructor Details

Course Instructor Name	Abdul Khadar A/Sabin T T			Emp.ID	1737	
Total Teaching Experience		No. of times taught this course				

C. Course Delivery

1	Course Plan was circulated among students before the start of course					
2	Total No of Modules/Chapters the course consists		Covered		%	
3	Total No of Classes Planned for the course		Classes Held		%	
4	Any reasons for non-coverage of 100 % syllabus (if not covered)					

D. Course Outcome(s) & University Examination Results

University Examination Results						119
1	Appeared	119	Pass	118	%Pass	99
2	Lost eligibility due to shortage of attendance			0	%	0
3	No. of students obtained minimum CIE marks			119	%	100

Grades obtained by the students (No. of students)

Grade Letter	S	A	B	C	D	E	E	Marks	Max.	Avg.			
Grade Point	10	9	8	7	6	4	0				CIE	40	37
No. of Students		35	49	29	5						SEE	60	37
% Students)		29	41	24	4						Total	100	74

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Course Title	MICROPROCESSORS AND EMBEDDED SYSTEMS				Course Code	C214	
Subject Code	18CS44	Semester	4	Section	A & B	Emp.ID	1737
Faculty Name	Abdul Khadar A/Sabin T T				No.students	119	

List of 10 Students scored Highest Marks (F)

Sl.	USN	NAME	Total_Marks	Rank	Remarks
1	1SJ19IS006	AKASH R	170	1	
2	1SJ19IS009	ANKUSHA J R	170	1	
3	1SJ19IS010	ANUSHA G	170	1	
4	1SJ19IS011	ARCHANA R	170	1	
5	1SJ19IS013	BALAGUNDLA ANVESH	170	1	
6	1SJ19IS018	BOMMINENI LAKSHMI RAMYA	170	1	
7	1SJ19IS022	CHANDANA S	170	1	
8	1SJ19IS023	CHARANYA P M	170	1	
9	1SJ19IS032	DHANUNJAYA REDDY SAI LAVANYA	170	1	
10	1SJ19IS033	DHANYA SURYAMATH	170	1	

List of 10 Students scored Lowest Marks (S)

Sl.	USN	NAME	Total_Marks	Rank	Remarks
1	1SJ19IS070	Mohammed Huzaifa B	110	11	
2	1SJ19IS082	Praful Prakash Kulkarni	110	11	
3	1SJ19IS080	Pavan Kumar P S	110	11	
4	1SJ19IS047	KALYAN K R	137	10	
5	1SJ19IS101	Shreyas M	140	9	
6	1SJ19IS106	Snehith Prasad C H	140	9	
7	1SJ19IS100	Shiva Prasad C	140	9	
8	1SJ19IS113	Swaroop N Swamy	140	9	
9	1SJ19IS099	Saqlain Ulla Khan A	140	9	
10	1SJ19IS123	Vikhyath P	140	9	

Remarks of Course Instructor

Signature of Course Instructor

Signature of HOD/DAC

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Course Title		MICROPROCESSORS AND EMBEDDED SYSTEMS				Course Code		C214	
Subject Code		18CS44	Semester	4	Section	A & B	Emp.ID		1737
Faculty Name		Abdul Khadar A/Sabin T T				No.students		119	
84	1SJ19IS090	Radhika P			Y	Y	Y	Y	Y
85	1SJ19IS091	Raksha M			Y	Y	Y	Y	Y
86	1SJ19IS092	S Jayanth			Y	Y	Y	Y	Y
87	1SJ19IS093	S N Rakesh			Y	Y	Y	Y	Y
88	1SJ19IS094	S P Vidya Sagar			Y	Y	Y	Y	Y
89	1SJ19IS095	Sahana D R			Y	Y	Y	Y	Y
90	1SJ19IS096	Sandhya D M			Y	Y	Y	Y	Y
91	1SJ19IS098	Sanjay M			Y	Y	Y	Y	Y
92	1SJ19IS099	Saqlain Ulla Khan A			Y	Y	Y	Y	Y
93	1SJ19IS100	Shiva Prasad C			Y	Y	Y	Y	Y
94	1SJ19IS101	Shreyas M			Y	Y	Y	Y	Y
95	1SJ19IS102	Shubhavarana N			Y	Y	Y	Y	Y
96	1SJ19IS103	Siddesh Gundagi			Y	Y	Y	Y	Y
97	1SJ19IS104	Sindhura N			Y	Y	Y	Y	Y
98	1SJ19IS105	Sneha G S			Y	Y	Y	Y	Y
99	1SJ19IS106	Snehith Prasad C H			Y	Y	Y	Y	Y
100	1SJ19IS107	Spoorthi S Suresh			Y	Y	Y	Y	Y
101	1SJ19IS108	Srinidhi B V			Y	Y	Y	Y	Y
102	1SJ19IS109	Suhail Khan I			Y	Y	Y	Y	Y
103	1SJ19IS110	Suhas A			Y	Y	Y	Y	Y
104	1SJ19IS111	Sujana Raghavendra S			Y	Y	Y	Y	Y
105	1SJ19IS113	Swaroop N Swamy			Y	Y	Y	Y	Y
106	1SJ19IS114	Swathi N			Y	Y	Y	Y	Y
107	1SJ19IS116	Tejas S Kumar			Y	Y	Y	Y	Y
108	1SJ19IS117	Tharun P C			Y	Y	Y	Y	Y
109	1SJ19IS118	Uday Kumar J B			Y	Y	Y	Y	Y
110	1SJ19IS119	Vandana K			Y	Y	Y	Y	Y
111	1SJ19IS120	Vasuki M			Y	Y	Y	Y	Y
112	1SJ19IS121	Vayalpad Mohammad Thouhid			Y	Y	Y	Y	Y
113	1SJ19IS122	Veeravalli Mahendra			Y	Y	Y	Y	Y
114	1SJ19IS123	Vikhyath P			Y	Y	Y	Y	Y
115	1SJ19IS124	Yarraguntla Chandana			Y	Y	Y	Y	Y
116	1SJ19IS125	Yashaswini H S			Y	Y	Y	Y	Y
117	1SJ19IS126	Yashaswini S			Y	Y	Y	Y	Y
118	1SJ19IS127	Matam Lal Bahudhur			Y	Y	Y	Y	Y
119	1SJ19IS128	RAKSHITHA			Y	Y	Y	Y	Y

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Subject Code		18CS44	Semester	4	Section	A & B	Emp.ID		1737
Faculty Name		Abdul Khadar A/Sabin T T				No.students		119	
41	1SJ19IS044	HITHAISHI A L			Y	Y	Y	Y	Y
42	1SJ19IS045	JAHNAVI D N			Y	Y	Y	Y	Y
43	1SJ19IS046	KALAVAA SAIDEEPA			Y	Y	Y	Y	Y
44	1SJ19IS047	KALYAN K R			Y	Y	Y	Y	Y
45	1SJ19IS048	KAVYA D			Y	Y	Y	Y	Y
46	1SJ19IS050	KAVYA D			Y	Y	Y	Y	Y
47	1SJ19IS051	KAVYA D R			Y	Y	Y	Y	Y
48	1SJ19IS052	KEERTHAN V			Y	Y	Y	Y	Y
49	1SJ19IS053	KIRAN S			Y	Y	Y	Y	Y
50	1SJ19IS054	LAKSHMI PRIYA Y L			Y	Y	Y	Y	Y
51	1SJ19IS055	LAVANYA A			Y	Y	Y	Y	Y
52	1SJ19IS056	LAXMIPATHI R			Y	Y	Y	Y	Y
53	1SJ19IS057	LITHISHA K J			Y	Y	Y	Y	Y
54	1SJ19IS058	MAKKAMGARI SREYA			Y	Y	Y	Y	Y
55	1SJ19IS059	MADDUR DINESH			Y	Y	Y	Y	Y
56	1SJ19IS060	MADHAVA K V			Y	Y	Y	Y	Y
57	1SJ19IS061	MADHAVANAND			Y	Y	Y	Y	Y
58	1SJ19IS062	MAHENDRA Y J			Y	Y	Y	Y	Y
59	1SJ19IS064	Manasa S			Y	Y	Y	Y	Y
60	1SJ19IS065	Manisha C			Y	Y	Y	Y	Y
61	1SJ19IS066	Meghana L C			Y	Y	Y	Y	Y
62	1SJ19IS067	Meghana N S			Y	Y	Y	Y	Y
63	1SJ19IS068	Meghashree C V			Y	Y	Y	Y	Y
64	1SJ19IS069	Modupalli Suneela			Y	Y	Y	Y	Y
65	1SJ19IS070	Mohammed Huzaifa B			Y	Y	Y	Y	Y
66	1SJ19IS071	Mounika D M			Y	Y	Y	Y	Y
67	1SJ19IS072	Mullaputi Praneeth			Y	Y	Y	Y	Y
68	1SJ19IS073	Navitha H A			Y	Y	Y	Y	Y
69	1SJ19IS074	Navya S			Y	Y	Y	Y	Y
70	1SJ19IS075	Navyashree A G			Y	Y	Y	Y	Y
71	1SJ19IS076	Nayana K			Y	Y	Y	Y	Y
72	1SJ19IS077	Nisha K M			Y	Y	Y	Y	Y
73	1SJ19IS078	Nithya Jyothi P M			Y	Y	Y	Y	Y
74	1SJ19IS079	Nithya S			Y	Y	Y	Y	Y
75	1SJ19IS080	Pavan Kumar P S			Y	Y	Y	Y	Y
76	1SJ19IS082	Praful Prakash Kulkarni			Y	Y	Y	Y	Y
77	1SJ19IS083	Prajwal P			Y	Y	Y	Y	Y
78	1SJ19IS084	Prakruthi C			Y	Y	Y	Y	Y
79	1SJ19IS085	Praveen S			Y	Y	Y	Y	Y
80	1SJ19IS086	Prekshitha D			Y	Y	Y	Y	Y
81	1SJ19IS087	Priya S			Y	Y	Y	Y	Y
82	1SJ19IS088	R Sai Abhiram			Y	Y	Y	Y	Y
83	1SJ19IS089	Rachan S H			Y	Y	Y	Y	Y

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Subject Code	18CS44	Semester	4	Section	A & B	Emp.ID	1737
Faculty Name	Abdul Khadar A/Sabin T T				No.students	119	

CO Analysis from -TEST - 3, in the Subject: 18CS44-Based on: TYPE-1, Academic Year 2020-21

Sl.	USN	Course Outcome Number	CO1	CO2	CO3	CO4	CO5	CO6
		Total Maximum Marks	20	40	30	20	20	40
1	1SJ19IS001	ABHIKUMAR R	Y	Y	Y	Y	Y	Y
2	1SJ19IS002	ADARSH K R	Y	Y	Y	Y	Y	Y
3	1SJ19IS004	ADARSH D R	Y	Y	Y	Y	Y	Y
4	1SJ19IS005	AKASH N	Y	Y	Y	Y	Y	Y
5	1SJ19IS006	AKASH R	Y	Y	Y	Y	Y	Y
6	1SJ19IS007	AMRUTHA S DUKANDAR	Y	Y	Y	Y	Y	Y
7	1SJ19IS008	ANDE NAGASHRI	Y	Y	Y	Y	Y	Y
8	1SJ19IS009	ANKUSHA J R	Y	Y	Y	Y	Y	Y
9	1SJ19IS010	ANUSHA G	Y	Y	Y	Y	Y	Y
10	1SJ19IS011	ARCHANA R	Y	Y	Y	Y	Y	Y
11	1SJ19IS012	B KIRAN	Y	Y	Y	Y	Y	Y
12	1SJ19IS013	BALAGUNDLA ANVESH	Y	Y	Y	Y	Y	Y
13	1SJ19IS014	BALIGOLLA MAHIDHAR	Y	Y	Y	Y	Y	Y
14	1SJ19IS015	BELDAR MANOGNA SAI SIMHA REDDY	Y	Y	Y	Y	Y	Y
15	1SJ19IS016	BHAVANI D	Y	Y	Y	Y	Y	Y
16	1SJ19IS017	BHOOMIKA R	Y	Y	Y	Y	Y	Y
17	1SJ19IS018	BOMMINENI LAKSHMI RAMYA	Y	Y	Y	Y	Y	Y
18	1SJ19IS019	CHANDAN G M	Y	Y	Y	Y	Y	Y
19	1SJ19IS020	CHANDAN K J	Y	Y	Y	Y	Y	Y
20	1SJ19IS021	CHANDAN R	Y	Y	Y	Y	Y	Y
21	1SJ19IS022	CHANDANA S	Y	Y	Y	Y	Y	Y
22	1SJ19IS023	CHARANYA P M	Y	Y	Y	Y	Y	Y
23	1SJ19IS024	CHAITHRA REDDY V	Y	Y	Y	Y	Y	Y
24	1SJ19IS025	CHETHANA C	Y	Y	Y	Y	Y	Y
25	1SJ19IS026	CHETHANA S	Y	Y	Y	Y	Y	Y
26	1SJ19IS028	DEEKSHA B M	Y	Y	Y	Y	Y	Y
27	1SJ19IS029	DEEPAK M	Y	Y	Y	Y	Y	Y
28	1SJ19IS030	DEEPTHISHREE S	Y	Y	Y	Y	Y	Y
29	1SJ19IS031	DEVRAJ PATIL	Y	Y	Y	Y	Y	Y
30	1SJ19IS032	DHANUNJAYA REDDY SAI LAVANYA	Y	Y	Y	Y	Y	Y
31	1SJ19IS033	DHANYA SURYAMATH	Y	Y	Y	Y	Y	Y
32	1SJ19IS034	DHRUTHI R	Y	Y	Y	Y	Y	Y
33	1SJ19IS035	G PAWAN NIKHIL	Y	Y	Y	Y	Y	Y
34	1SJ19IS036	GERIGI YOGA SAI GANESH	Y	Y	Y	Y	Y	Y
35	1SJ19IS037	GORAVA DEVENDRA	Y	Y	Y	Y	Y	Y
36	1SJ19IS038	GOVARDHANA J A	Y	Y	Y	Y	Y	Y
37	1SJ19IS039	GOWTHAM K A	Y	Y	Y	Y	Y	Y
38	1SJ19IS041	GUNASHEKHAR G	Y	Y	Y	Y	Y	Y
39	1SJ19IS042	H HARI RAJ	Y	Y	Y	Y	Y	Y
40	1SJ19IS043	HEMANTH KUMAR N	Y	Y	Y	Y	Y	Y

SJCIT/NBA/
CO-REPT/
2020-21

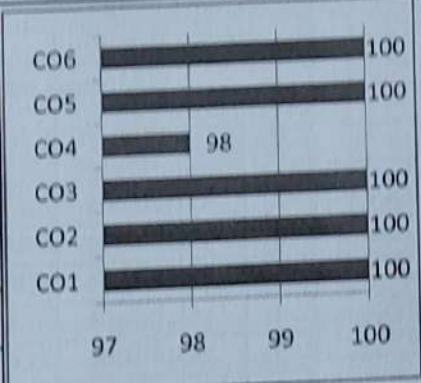


S J C INSTITUTE OF TECHNOLOGY
Chickballapur - 562 101
Department of Information Science & Engineering

Course Title	MICROPROCESSORS AND EMBEDDED SYSTEMS				Course Code	C214	
Subject Code	18CS44	Semester	4	Section	A & B	Emp.ID	1737
Faculty Name	Abdul Khadar A/Sabin T T				No.students	119	

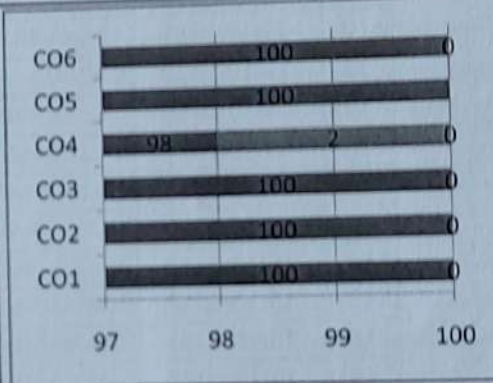
CO Attainment from -TEST - 3, in the Subject: 18CS44-Based on: TYPE-1, Academic Year 2020-21

Sl.	CO Number	Sum	T_Std	Av-AT	TS(=3)	AT,%	Ac_AT	ATNT
CO1	C214.1	357	119	3	119	100	3	YES
CO2	C214.2	357	119	3	119	100	3	YES
CO3	C214.3	357	119	3	119	100	3	YES
CO4	C214.4	355	119	3	117	98	3	YES
CO5	C214.5	357	119	3	119	100	3	YES
CO6	C214.6	357	119	3	119	100	3	YES



Distribution of CO Attainment from -TEST - 3, in Subj: 18CS44-Based on: TYPE-1, ACY:2020-21

Sl.	CO Number	3	%	2	%	1	%
CO1	C214.1	119	100		0		0
CO2	C214.2	119	100		0		0
CO3	C214.3	119	100		0		0
CO4	C214.4	117	98	2	2		0
CO5	C214.5	119	100		100		100
CO6	C214.6	119	100		0		0



Remarks of Course Instructor

(This area is currently blank for remarks.)

Signature of HOD/DAC

Signature of Course Instructor

(Handwritten signature of HOD/DAC)

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SJCIT/NBA/
COURSE/
2020-21



S J C INSTITUTE OF TECHNOLOGY
Chickballapur - 562 101
Department of Information Science & Engineering

Course Information

Programme Name:	Information Science & Engineering					
Academic Year:	2020-21	Semester:	4	Section:	A & B	Subject Type:
Course Title:	MICROPROCESSORS AND EMBEDDED SYSTEMS					
Course Instructor Name:	Abdul Khadar A/Sabin T T				Class Strength:	
Subject Code:	18CS44	Course No:	4	Course ID:	C214	119

Scheme of Teaching & Marks

Contact Hr/Week:	4	Lecture Hours (Hr.):	4	Tutorials (Hr.):	0
Max.CIE Marks:	40	Max. SEE Marks:	60	Total Max.Marks:	100
Min.CIE Marks:	19	Min.SEE Marks:	21	Total Min.Marks:	40
Final CIE (IA) Marks:	40	Assignment Marks:	10	Test Marks:	30

Threshold Values for Attainment Calculation

Final CO Attainment

Attainment level	Threshold Values				Final CO Attainment (Percentage Contribution, %)				
	3	%	2	%	1	%	CIE	SEE	CES
Internal Assessment	>=	70	>=	60	>=	50	40	50	10
SE Examination	>=	60	>=	50	>=	40	-	-	-

Statements of Course Outcomes

No.of CO's

6 Target(%) BL

CO	Description	Target(%)	BL
C214.1	Acquire the knowledge of the architecture features and instructions of ARM microcontroller	60	
C214.2	Apply the knowledge gained for programming ARM for different applications and interface external devices and IO with ARM MC	60	
C214.3	Interpret the basic h/w components & their selection method based on the characteristics and attributes of an embedded system	60	
C214.4	Develop the h/w & s/w co-design & firmware design approaches	60	
C214.5	Demonstrate the need of RTOS for embedded system applications	60	
C214.6	Present a seminar on important & advanced features of ARM controller	60	

Semester End Exam. (SEE) Target(%)	60	Course End Survey(CES) Target(%)	70
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CO-PO Mapping Table (In the scale of 3)

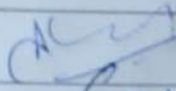
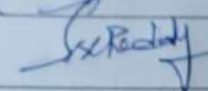
CO-PSO Mapping Table

CO/PO	CO-PO Mapping (Scale of 3)												CO-PSO Mapping				
	1	2	3	4	5	6	7	8	9	10	11	12	CO/PSO	1	2	3	4
C214.1	3	1											C214.1		3		
C214.2	3	1	1								2		C214.2		3		
C214.3		3		1							1		C214.3		2		
C214.4	1	1	3										C214.4	2	2		
C214.5			1	3							1		C214.5				
C214.6									2	3	1	2	C214.6	1	1		
Total	7	6	5	4					2	3	1	6	Total	3	11		

INTERNAL/ASSIGNMENT/QUIZ SCHEDULE

TEST and QUIZ		COs and Portions Covered		ASSIGNMENT	
Test# and Quiz#	DATE	CO	Modules	Assignment#	DATE
T1 & Q1	22/5	CO1, CO2	1,2	A1	3/5, 31/5
T2 & Q2	21/6	CO2, CO3	2,3	A2	14/6, 6/7
T3 & Q3	20/8	CO4, CO5	4,5	A3	23/7

SUMMARY

Signatures With Date	Faculty: 	Total #HOURS	Allotted	Taken
	HOD: 			
Remarks				

ENCLOSURES

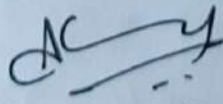
1. Syllabus
2. CO Attainment
3. Gap Analysis
4. Special lectures/talks arranged if any

Feedback by PAC

All COs & POS are attained and targets are achieved. Can improve by targets for the coming Academic Year.



Faculty



Course coordinator



PAC

HOD

<i>Module -4</i>			
<i>Q. No.</i>	<i>Questions</i>	<i>Bloom's LL</i>	<i>COs</i>
1	Explain the characteristics of Embedded systems	L2	CO4
2	Explain the operational and non-operational quality attributes of Embedded systems.	L2	CO4
3	Apply the operation of Washing Machine as Application-Specific Embedded system. And explain with the functional block diagram,	L3	CO4
4	Explain the fundamental issues in Hardware Software co-design	L2	CO4
5	Design & explain FSM model for automatic seat belt warning system.	L4	CO4
6	Explain two basic approaches for designing Embedded Firmware.	L2	CO4
7	Explain Quality attributes of embedded system?	L2	CO4
8	With neat sketch explain various computational models in embedded system?	L2	CO4
9	Explain the embedded Assembly language firmware development languages.	L2	CO4
10	Explain the embedded High level language based development.	L2	CO4

<i>Module -5</i>			
<i>Q. No.</i>	<i>Questions</i>	<i>Bloom's LL</i>	<i>COs</i>
1	Explain two different approaches for building an operating system kernel.	L2	CO4
2	Define the terms Task, Process and Threads? Explain the Process structure, process states and state transitions.	L2	CO4
3	Explain the different types of multitasking.	L2	CO4
4	Explain the task communication/synchronization issues	L2	CO4
5	Explain the functional and non-functional requirements to be considered while choosing an RTOS for an Embedded design.	L2	CO4
6	Explain basics of operating system?	L2	CO4
7	Explain structure of process?	L2	CO4
8	What is scheduling? Explain the various for scheduling algorithms in RTOS?	L1	CO4
9	What is semaphore? Explain various types of semaphores in RTOS?	L1	CO4
10	Explain integration of hardware and firmware design of embedded system.	L2	CO4

Note:

1. Questions shall be framed by consolidating comprehensively from the following sources
 - Exercise problems of text books/ references
 - Previous year question VTU exam Question paper. (Mark the year/exam beside the question)
 - Questions by Experts during Interview/Academic Audit
 - Internet sources/ other Universities examination question papers.
 - Own / experience.
 - Gate questions mentioning the year.
2. Questions shall follow all the Bloom's learning levels with appropriate action verbs
3. There shall be a total of 50 questions considering 10 questions from each module, of which, 3 questions each at L1 and L2, 2 questions at L3, 1 question each at L4 and L5/L6.
4. Ensure the coverage of all Cos.

<i>Module -2</i>			
<i>Q. No.</i>	<i>Questions</i>	<i>Bloom's LL</i>	<i>COs</i>
1	List and explain arithmetic instructions with respect to the ARM processor	L2	CO2
2	Illustrate the load & store instructions with respect to the Single Register Transfer with example for each	L2	CO2
3	Explain briefly co-processor instructions of ARM processor.	L1	CO2
4	Design ARM assembly language program to perform the addition and multiplication of two 32 bit numbers.	L4	CO2
5	Define instruction scheduling? Explain the rules summarizing the cycle timings for common instruction classes on the ARM9TDMI.	L2	CO2
6	Apply the scheduling of following instructions with respect to the ARM9TDMI pipeline implementation, i) STR ii) LDRH iii) B Label	L3	CO2
7	Explain barrel shift operations in ARM processor.	L2	CO2
8	Explain Branch instructions.	L2	CO2
9	Explain briefly the loading constants.	L2	CO2
10	Explain briefly program status register instructions with syntax and example	L2	CO2

<i>Module -3</i>			
<i>Q. No.</i>	<i>Questions</i>	<i>Bloom's LL</i>	<i>COs</i>
1	Differentiate Embedded systems and General purpose computing systems	L2	CO3
2	What are the major application areas of Embedded systems? Explain the various purposes of embedded systems.	L1	CO3
3	Explain the system core of the Embedded systems.	L1	CO3
4	Illustrate the application of the interfacing of following I/O subsystems with Embedded systems i) 7-Segmnet LED Display ii) Stepper Motor.	L3	CO3
5	Write a short note on onboard communication interfaces in Embedded systems	L2	CO3
6	Explain instruction pipelining with load and store operations in embedded system.	L2	CO3
7	Explain sensors and actuators with I/O subsystem.	L2	CO3
8	Explain the followings. a. LED b. Opt couplers c. Relay d. Push button switches	L2	CO3
9	Explain communication interfaces. a. I2C b. Serial peripheral interface, c. UART	L2	CO3
10	Explain other system components in embedded system. a. Reset circuits b. Real time clock c. Watchdog Timer	L2	CO3



Estd: 1986

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Sri Adichunchanagiri Shikshana Trust ®

SJC INSTITUTE OF TECHNOLOGY

Chickballapur – 562 101

Department of Information Science & Engineering

QUESTION BANK

SUBJECT TITLE	Microcontroller and Embedded Systems		
SUBJECT TYPE	CORE / ELECTIVE		
SUBJECT CODE	18CS44		
ACADEMIC YEAR	2021 (EVEN SEMESTER)	BATCH	2018-2022
SCHEME	2018, CBCS		
SEMESTER	4 th 'B'		
FACULTY NAME and DESIGNATION	ABDUL KHADAR A, Assistant Professor		

Module -1

Q. No.	Questions	Bloom's LL	COs
1	Differentiate between RISC and CISC processors.	L2	CO1
2	Explain the major design rules to implement the RISC philosophy	L1	CO1
3	Explain ARM core data flow model with neat diagram.	L1	CO1
4	Explain the programmer's model of ARM processors with complete register sets available.	L1	CO1
5	With the help of bit layout diagram illustrate current program status register of ARM.	L2	CO1
6	Explain briefly the processor modes for ARM processor.	L1	CO1
7	Explain detail, the pipeline concept for ARM processor.	L1	CO1
8	Explain briefly the interrupt and the vector table.	L1	CO1
9	Discuss the core extensions for ARM processor.	L1	CO1
10	Explain ARM bus technology.	L1	CO1

Note:

1. Questions shall be framed by consolidating comprehensively from the following sources
 - Exercise problems of text books/ references
 - Previous year question VTU exam Question paper. (Mark the year/exam beside the question)
 - Questions by Experts during Interview/Academic Audit
 - Internet sources/ other Universities examination question papers.
 - Own / experience.
2. Questions shall follow all the Bloom's learning levels with appropriate action verbs
3. There shall be a total of 25 questions considering 5 questions from each module, of which, 3 questions at L3, 2 questions each at L4/L5.
4. Ensure the coverage of all COs
5. Rubrics to be specified for all assignment questions.

<i>Module -3</i>			
<i>Q. No.</i>	<i>Questions</i>	<i>Bloom's LL</i>	<i>COs</i>
1	Differentiate Embedded systems and General purpose computing systems	L2	CO3
2	What are the major application areas of Embedded systems? Explain the various purposes of embedded systems.	L1	CO3
3	Explain the system core of the Embedded systems.	L1	CO3
4	Illustrate the application of the interfacing of following I/O subsystems with Embedded systems i) 7-Segmnet LED Display ii) Stepper Motor.	L3	CO3
5	Write a short note on onboard communication interfaces in Embedded systems	L2	CO3

<i>Module -4</i>			
<i>Q. No.</i>	<i>Questions</i>	<i>Bloom's LL</i>	<i>COs</i>
1	Explain the characteristics of Embedded systems	L2	CO4
2	Explain the operational and non-operational quality attributes of Embedded systems.	L2	CO4
3	Apply the operation of Washing Machine as Application-Specific Embedded system. And explain with the functional block diagram,	L3	CO4
4	Explain the fundamental issues in Hardware Software co-design	L2	CO4
5	Design & explain FSM model for automatic seat belt warning system.	L4	CO4
6	Explain two basic approaches for designing Embedded Firmware.	L4	CO4

<i>Module -5</i>			
<i>Q. No.</i>	<i>Questions</i>	<i>Bloom's LL</i>	<i>COs</i>
1	Explain two different approaches for building an operating system kernel.	L2	CO4
2	Define the terms Task, Process and Threads? Explain the Process structure, process states and state transitions.	L2	CO4
3	Explain the different types of multitasking.	L2	CO4
4	Explain the task communication/synchronization issues	L2	CO4
5	Explain the functional and non-functional requirements to be considered while choosing an RTOS for an Embedded design.	L2	CO4



Estd: 1986

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Sri Adichunchanagiri Shikshana Trust ®

SJC INSTITUTE OF TECHNOLOGY

Chickballapur – 562 101

Department of Information Science & Engineering ASSIGNMENT

SUBJECT TITLE	Microcontroller and Embedded Systems		
SUBJECT TYPE	CORE / ELECTIVE		
SUBJECT CODE	18CS44		
ACADEMIC YEAR	2021 (EVEN SEMESTER)	BATCH	2018-2022
SCHEME	2018, CBCS		
SEMESTER	4 th 'B'		
FACULTY NAME and DESIGNATION	ABDUL KHADAR A, Assistant Professor		

Module -1

Q. No.	Questions	Bloom's LL	COs
1	Differentiate between RISC and CISC processors.	L2	CO1
2	Explain the major design rules to implement the RISC philosophy	L1	CO1
3	Explain ARM core data flow model with neat diagram.	L1	CO1
4	Explain the programmer's model of ARM processors with complete register sets available.	L1	CO1
5	With the help of bit layout diagram illustrate current program status register of ARM.	L2	CO1

Module -2

Q. No.	Questions	Blooms LL	COs
1	List and explain arithmetic instructions with respect to the ARM processor	L2	CO2
2	Illustrate the load & store instructions with respect to the Single Register Transfer with example for each	L2	CO2
3	Explain briefly co-processor instructions of ARM processor.	L1	CO2
4	Design ARM assembly language program to perform the addition and multiplication of two 32 bit numbers.	L4	CO2
5	Define instruction scheduling? Explain the rules summarizing the cycle timings for common instruction classes on the ARM9TDMI.	L2	CO2
6	Apply the scheduling of following instructions with respect to the ARM9TDMI pipeline implementation, i) STR ii) LDRH iii) B Label	L3	CO2

- 1)MVN R0,R1 2)ORR R0,R1,R2 3)MOV R0,R1,LSL #4 4)BIC R2,R0,R1
5) ADD R0,R1,R1,LSR #4 6)MOV R2,R1, LSR #4

7. Write an Assembly level program for find a factorial of number and explain the execution steps

8 Write an Assembly level program for multiply two 16 bit number and store the result into memory location 0x4000000c

9 .Precondition r0=0x0 ,r1=0x4000

Mem32[0x4000]=0xffffffff

Mem32[0x4004]=0x11111111

Find the post condition of registers r0 and r1 after executing following instructions

- i) LDR r0,[r1, #4]
- ii) LDR r0,[r1, #4]
- iii) LDR r0,[r1], #4

SUR

S.J.C Institute of Technology

Department of Information Science and Engineering

Subject Name & Code: MC&ES-18CS44

Semester: 4th 'A' & 'B'

TUTORIAL -I

MODULE-I

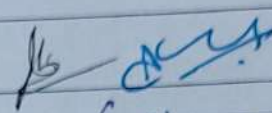
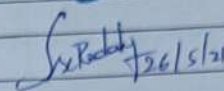
1. Differentiate between a) microprocessor and microcontroller b) RISC and CISC.
2. Explain a) the RISC design philosophy b) ARM design philosophy.
3. With a neat diagram explain ARM based embedded system (microcontroller) and also explain the instruction set for embedded system. / Explain the architecture of a typical embedded device based on a ARM core with a neat diagram
4. Explain with a neat diagram abstract component that make up an ARM core/ARM core data flow model/programmer's model of ARM processor
5. Define bank register? Explain various registers available in ARM (complete ARM register set).
6. Explain all the fields of a generic program status register.
7. Explain the pipeline executing characteristics.
8. What is an interrupt? Explain vector table.
9. Explain various core extensions of ARM.
10. Describe the various modes of operation and various states of ARM processor
11. List and explain various processor modes of ARM processor
12. Discuss the following with diagram i)- Von Neuman Architecture with cache
ii) Harward architecture with TCM

MODULE-5

1. Explain the instruction with syntax and example.
1)MVN 2)BIC 3)RSB 4)CMN 5)SMLAL 6)BL 7)LDR 8)MLA 9)ADC 10)TEQ
2. With help of a neat diagram explain the use of barrel shifter and its operation.
3. Explain with syntax, various multiplication instructions.
4. Explain single register transfer and its addressing modes.
6. Precondition R0=0x10101010 R2=0x00000000 R1=0xFFFFFFFF Write down the post condition after R0,R1,R2 after

4) ADD R0,R1,R1,LSR #4		5)MOV R2,R1, LSR #4			
OR					
10.	Pre condition r0=0x0 ,r1=0x4000 Mem32[0x4000]=0xffffffff Mem32[0x4004]=0x11111111 Mem32[0x4008]=0x22222222 Find the post condition of registers r0 and r1 after executing following instructions i) LDR r0,[r1, #8] ii) LDR r0,[r1, #8] iii) LDR r0,[r1], #8	CO-2	10	L3	

Internal Test Question paper format – 2018 Scheme

Name of the staff/s: Abdul khaddar A . Sabin T T
Date: 26-5-2021Signature: Reviewer's Signature: S.J.C Institute of Technology
Department of Information Science and Engineering

Test: I

Semester: IV

Subject: MICRO CONTROLLER AND EMBEDDED SYSTEMS (18CS44)

Section: A & B

Date: 28-5-2021

Max Marks: 50

Answer the following questions

Sl. No	Questions	CO	Marks	Level
1.	With a neat diagram explain ARM basis embedded system (microcontroller) and also explain the instruction set for embedded system.	CO-1	10	L2
OR				
2.	Explain with a neat diagram abstract component that make up an ARM core/	CO-1	10	L2
3.	Define Banked register? Explain various registers available in ARM	CO-1	10	L2
OR				
4.	What is mean by pipelining? Explain the pipeline executing characteristics	CO-1	10	L2
5.	Describe the various modes of operation and various states of ARM processor	CO-1	10	L2
OR				
6.	Explain various core extensions of ARM.	CO-1	10	L2
7.	i) Explain with example single register transfer and its addressing modes. ii) Explain the instruction with syntax and example a.BIC b.CMP	CO-2	6 4	L2
OR				
8.	i) With help of a neat diagram explain the use of barrel shifter and its operation ii) Explain the instruction with syntax and example i.MVN ii RSB	CO-2	6 4	L2
9.	Precondition R0=0x00000000 R2=0x00000000 R1=0xFFFFFFFF write down the post condition after R0,R1,R2 After Execution of following instruction 1)MVN R0,R1 2)MOV R0,R1,LSL #4 3)BIC R2,R0,R1	CO-2	10	L3

Subject Title: MIES

Subject Code: 12CS44

Question Number	Solution	Marks Allocated
10	<p>1) $r_0 = 0x22222222$ $r_1 = 0x4008$ - Pre index with write back - base register is updated.</p> <p>2) $r_0 = 0x22222222$ $r_1 = 0x4000$ - "PreIndex" - base register is not updated</p> <p>3) $r_0 = 0xffffffff$ $r_1 = 0x4008$ - Post Index.</p> <p style="text-align: right;">=</p>	<p>4M</p> <p>3M</p> <p>3M</p> <p>[4+3+3] $\rightarrow 10M$</p>

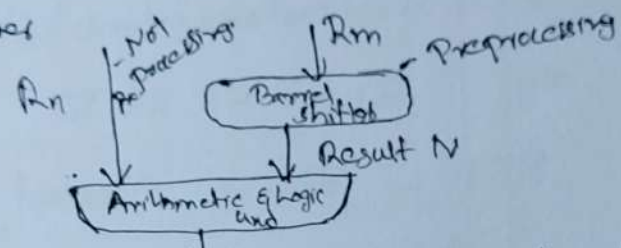
SJP

||jai Sri Gurdev||
S J C Institute of Technology
Department of Information Science and Engineering

Semester: 4th

Test Scheme & Solutions

Subject Title & Code: - Micro Controller & Embedded System
18CS44

Question Number	Solution	Marks Allocated
8	<p>g) Barrel shifter</p>  <p>Barrel shifter is a hardware component within a processor which preprocesses one of the operand of ALU --</p> <p>Barrel shifter operation</p> <ol style="list-style-type: none"> ① logical shift left - LSL ② logical shift right - LSR ③ Arithmetic right shift - ASR ④ Rotate right - ROR ⑤ Rotate right extend - RAX 	<p align="right">2M</p>
9	<p>h) MVN - Move the not of 32 bit value into a register. Rd = N</p> <p>Syntax <instruction> {<cond>} {S} Rd, N</p> <p>eg: MVN MVN R1, R2</p> <p>CMP → compare; flag set as a result of Rn - N</p> <p>Syntax - <instruction> {<cond>} Rn, N</p> <p>eg: CMP R1, R2</p>	<p align="right">2M</p>

SJB

Explanation with example

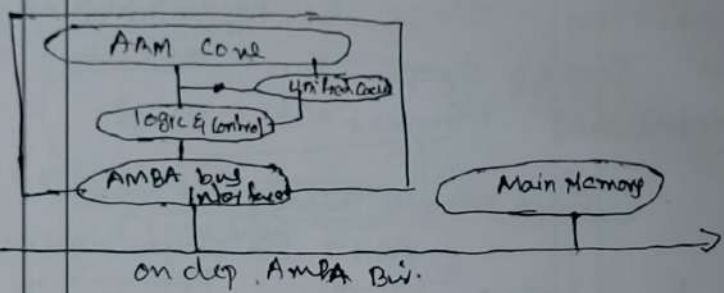
AM.

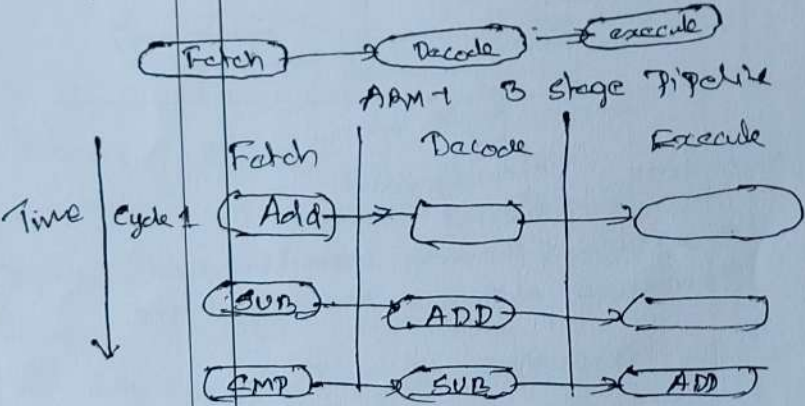
(2+2) = 4M



Subject Title: **MES**

Subject Code: **18CS44**

Question Number	Solution	Marks Allocated																
6	<p>Core - Extensions</p> <p>① Cache and Tightly Coupled memory</p>  <p>② Memory Management</p> <ul style="list-style-type: none"> ① - Non protected memory ② MPU - (Memory Protection unit) ③ MMU - Memory Management unit <p>③ Co-Processors</p>	<p>4M</p> <p>3M</p> <p>3M</p>																
7	<p>Single register transfer</p> <p>Syntax</p> <p><LDR> {<cond>} Rd, addressing ← load</p> <p><STR> {<cond>} Rd, addressing.</p> <p>LDR & STR for load and store 32 bit data.</p> <p>variants are LDRB, LDRH, STRB, STRH</p> <p>eg: LDR R1, (R2) → 2M</p> <p>STR R3, (R4) → explain.</p> <table border="0"> <thead> <tr> <th>Index Method</th> <th>Data</th> <th>Base Address</th> <th>Example</th> </tr> </thead> <tbody> <tr> <td>Preindex with write back</td> <td>mem[base+offset]</td> <td>base+offset</td> <td>LDR R0, [R1, #4]</td> </tr> <tr> <td>Preindex</td> <td>mem[base+offset]</td> <td>not updated</td> <td>LDR R0, [R1, #4]</td> </tr> <tr> <td>Post index</td> <td>mem[base]</td> <td>base+offset</td> <td>LDR R0, [R1], #4</td> </tr> </tbody> </table>	Index Method	Data	Base Address	Example	Preindex with write back	mem[base+offset]	base+offset	LDR R0, [R1, #4]	Preindex	mem[base+offset]	not updated	LDR R0, [R1, #4]	Post index	mem[base]	base+offset	LDR R0, [R1], #4	<p>2M</p> <p>5M</p>
Index Method	Data	Base Address	Example															
Preindex with write back	mem[base+offset]	base+offset	LDR R0, [R1, #4]															
Preindex	mem[base+offset]	not updated	LDR R0, [R1, #4]															
Post index	mem[base]	base+offset	LDR R0, [R1], #4															

Question Number	Solution	Marks Allocated
4.	<p>Pipeline is a mechanism to speed up the execution, which divide the execution steps into smaller phases and these steps can execute in a independent manner.</p> <p style="text-align: center;">ARM 3 stage Pipeline</p>  <p>Pipelined instruction sequence</p> <p>Explain pipeline execution characteristics</p> <ul style="list-style-type: none"> ① ARM Pipeline has not processed an instruction until it passes completely through the execute stage. ② PC always point to the address of the instruction plw 8 	<p>3M.</p> <p>2M</p> <p>5M</p>
5.	<p>ARM Processor mode → explanation</p> <ul style="list-style-type: none"> 1- Abort 2- Fast interrupt request 3- Interrupt request 4- Supervisor 5- System 6- Undefined 7- user <p style="text-align: right;">State of ARM</p> <ul style="list-style-type: none"> 1- ARM state 2- Thumb state 3- Jazelle state 	<p>7M</p> <p>3M</p> <p>7+3 → 10M</p>

SJCIT

Question Number	Solution	Marks Allocated
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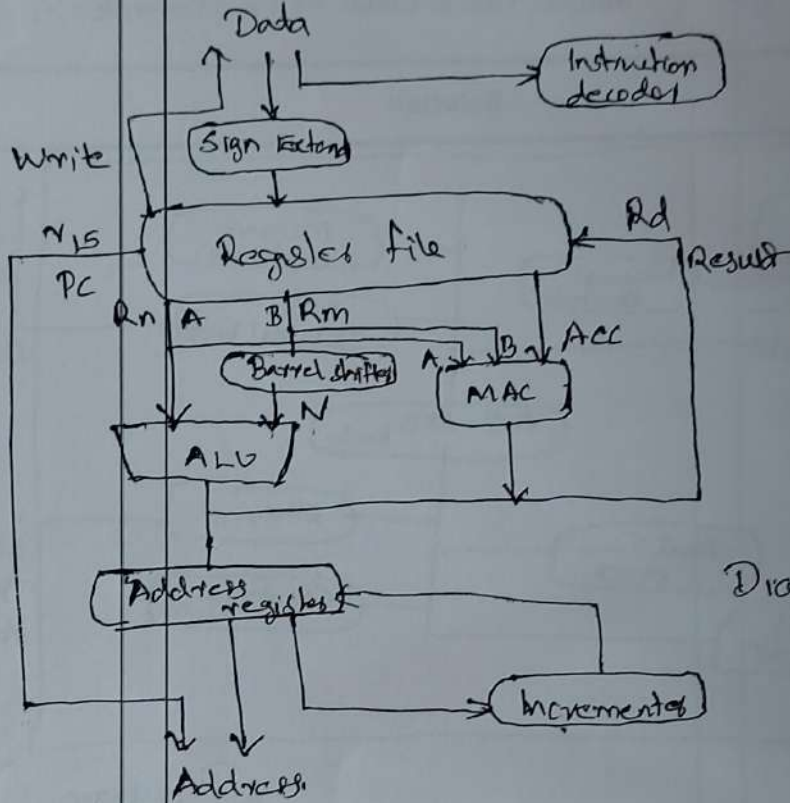
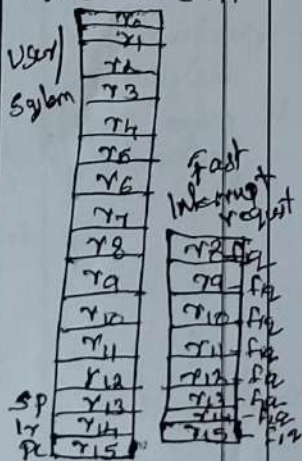


Diagram 5M.

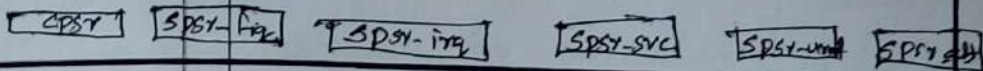
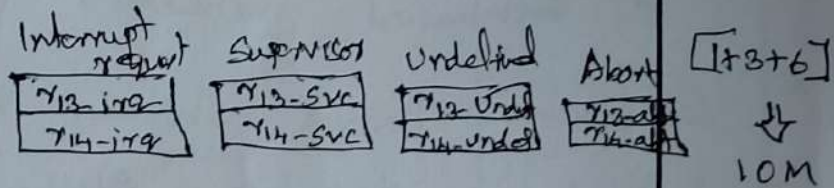
3.

There are 37 registers in register file. In that 20 registers are hidden from a program at different times. These registers are known as Banked registers. 1M



- Explain various registers
- Mode of CPSR, SPSR 3M

Diagram - 6M



||jai Sri Gurdev||
S J C Institute of Technology
Department of Information Science and Engineering

Test I Scheme & Solutions

Subject Title & Code: Micro Controller & Embedded Systems 18CS44

Semester: 4th - 'A' & 'B'

Question Number	Solution	Marks Allocated
1	<p align="right">Diagram</p> <p>Explanation of ① ARM Processor ② Controller ③ Peripheral ④ Bus</p> <ul style="list-style-type: none"> - Instruction Set for embedded system 1- Variable cycle execution for certain instructions 2- Inline barrel shifter leading to more complex instructions 3- Thumb - 16 bit instruction set 4- Conditional execution 5- Enhanced instruction <p>2. Explain - Barrel shifter, Register file decoder, ALU, MAC and instruction internal functioning of an ARM processor</p>	<p align="right">4M</p> <p align="right">2M</p> <p align="right">4M</p> <p align="right">4+2+4=10</p> <p align="right">5M</p>

S.J.C Institute of Technology

Department of Information Science and Engineering

Subject Name & Code: MCRES-18CS44

Semester: 4th 'A' & 'B'

TUTORIAL -II

- 1) Explain in detail multiple register transfer instruction and its addressing modes and demonstrate the execution of $LDHRL$ and $LDHL$ with suitable example 10m
- 2) with suitable example demonstrate the stack operations 10m
- 3) Illustrate the following instruction with syntax and example a) $SWAP$ b) DDI c) $MRCRMSR$ 10m
- 4) Write a code to find the factorial of a given number and list down the execution steps 10m
- 5) Explain briefly the different classification of Embedded systems 10m
- 6) Explain various purposes of Embedded systems and discuss the various application areas of it 10m
- 7) Differentiate between i) Microprocessor and Microcontrollers ii) $RISC$ and $CISC$ 10m
- 8) Explain different memory technologies and memory types used in Embedded systems development 10m
- 9) Analyse the role of input/output subsystems of an Embedded system 10m
- 10) Enumerate different communication interfaces of an embedded system 10m
- 11) Write a note about i) Bluetooth ii) Zigbee 10m
- 12) Explain different onboard communication in brief 10m
- 13) Explain the operation of i) Stepper motor ii) matrix keyboard 10m
- 14) List and explain various external interfaces 10m

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Subject Title: MES

Subject Code: 18CS44

Question Number	Solution	Marks Allocated																									
	<p>wave step - only one phase is energised at a time</p> <table border="1" data-bbox="295 459 1173 772"> <thead> <tr> <th>Step</th> <th>Coil A</th> <th>Coil B</th> <th>Coil C</th> <th>Coil D</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>H</td> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>2</td> <td>L</td> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>3</td> <td>L</td> <td>L</td> <td>H</td> <td>L</td> </tr> <tr> <td>4</td> <td>L</td> <td>L</td> <td>L</td> <td>H</td> </tr> </tbody> </table>	Step	Coil A	Coil B	Coil C	Coil D	1	H	L	L	L	2	L	H	L	L	3	L	L	H	L	4	L	L	L	H	2
Step	Coil A	Coil B	Coil C	Coil D																							
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3	L	L	H	L																							
4	L	L	L	H																							
	<p>Half step - uses the combination of wave and full step. It has highest torque & stability</p>	2M																									
10	<p>Bluetooth - low cost, low power, short range wireless technology for data and audio communication. It operates 2.4GHz radio frequency spectrum and FHSS technique for communication.</p> <p>It support data rate of 1 Mbps to 24 MBps</p> <p>- Two part. Physical link part and protocol part.</p> <p>WiFi - popular communication technique for networked communication of devices. It follows IEEE 802.11 standard. It support IP based communication. Each device is identified by IP address. Operate 2.4GHz or 5GHz at radio frequency.</p>	3M																									



Subject Title: MES

Subject Code: 18CS44

Question Number	Solution	Marks Allocated																									
	<p>Wave step - only one phase is energised at a time</p> <table border="1" data-bbox="375 526 1189 817"> <thead> <tr> <th>Step</th> <th>Coil A</th> <th>Coil B</th> <th>Coil C</th> <th>Coil D</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>H</td> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>2</td> <td>L</td> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>3</td> <td>L</td> <td>L</td> <td>H</td> <td>L</td> </tr> <tr> <td>4</td> <td>L</td> <td>L</td> <td>L</td> <td>H</td> </tr> </tbody> </table>	Step	Coil A	Coil B	Coil C	Coil D	1	H	L	L	L	2	L	H	L	L	3	L	L	H	L	4	L	L	L	H	2
Step	Coil A	Coil B	Coil C	Coil D																							
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10	<p>Bluetooth - low cost, low power, short range wireless technology for data and audio communication. It operates 2.4GHz radio frequency spectrum and FHSS technique for communication. It support data rate of 1Mbps to 24Mbps.</p> <p>Two part - Physical link part and protocol part.</p> <p>WiFi - popular communication technique for networked communication of devices. It follows IEEE 802.11 standard. It support IP based communication. Each device is identified by IP address. Operate 2.4GHz or 5GHz at 20MHz or 40MHz spectrum.</p>	3M																									

LR



Subject Title: MES

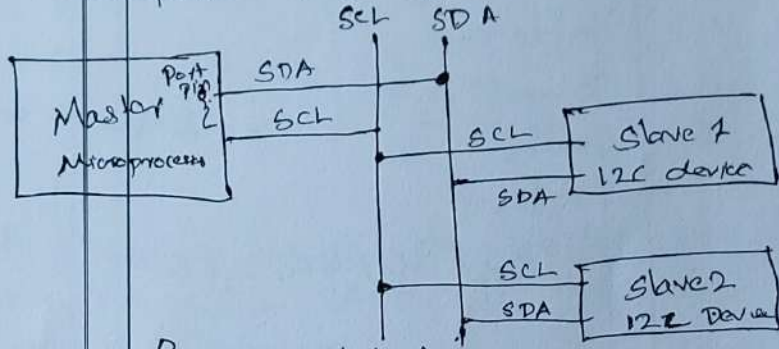
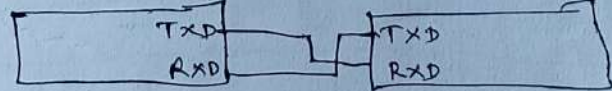
Subject Code: 18C544

Question Number	Solution	Marks Allocated																									
8	<p>External Communication Interfaces.</p> <ol style="list-style-type: none"> 1- RS-232 and RS 485 2- Universal Serial bus (USB) 3- IEEE 1394 (Fire wire) 4- Infrared 5- Blue Tooth 6. Wifi 7- Zigbee 8- GPRS, 3G, 4G, LTE 	<p>Explain any five - $5 \times 2 = 10$</p>																									
9.	<p>Stepper motor is an electro mechanical device which generates discrete displacement in response to discrete signals.</p> <p>Based on the coil winding arrangement a 2 phase stepper motor is classified into two</p> <ol style="list-style-type: none"> 1- Unipolar 2- Bipolar <p>Full Step - Both phases are energized simultaneously</p> <table border="1" data-bbox="371 1570 1289 1966"> <thead> <tr> <th>Step</th> <th>Coil A</th> <th>Coil B</th> <th>Coil C</th> <th>Coil D</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>H</td> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>2</td> <td>L</td> <td>H</td> <td>H</td> <td>L</td> </tr> <tr> <td>3</td> <td>L</td> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>4</td> <td>H</td> <td>L</td> <td>L</td> <td>H</td> </tr> </tbody> </table>	Step	Coil A	Coil B	Coil C	Coil D	1	H	H	L	L	2	L	H	H	L	3	L	L	H	H	4	H	L	L	H	<p>3</p> <p>3</p>
Step	Coil A	Coil B	Coil C	Coil D																							
1	H	H	L	L																							
2	L	H	H	L																							
3	L	L	H	H																							
4	H	L	L	H																							



Subject Title: MRS

Subject Code: 18CS44

Question Number	Solution	Marks Allocated
7	<p>Onboard Communication Interface.</p> <p>1) Intra Integrated Circuit Bus (I²C)</p> <ul style="list-style-type: none"> * Synchronous, * bi directional half duplex. * Comprise two line SCL & SDA  <p>I²C bus Interface.</p> <p>2) Serial peripheral Interface bus (SPI bus)</p> <ul style="list-style-type: none"> - Synchronous, bi directional, Full duplex. 4 wire serial interface. signals are MOSI - Master out slave in MISO - Master in slave out SCLK - Serial clock. SS → slave select. <p>3) Universal Asynchronous receiver & Transmitter (UART)</p> <ul style="list-style-type: none"> * no clock signal required * It work based on pre defined agreement  <p>TXD - Transmitter line RXD - receiver line</p> <p>4) 1-wire interface - only single signal line DA is used</p> <p>5) Parallel Interface</p>	<p>3M</p> <p>2M</p> <p>2M.</p> <p>1M</p> <p>2M</p>

SJP

Subject Title: MES

Subject Code: 18CS44

Question Number	Solution	Marks Allocated
	<p>SWI -</p> <p>$lv_svc = \text{address of instruction followed by SWI}$</p> <p>$SPSR_svc = CPSR$</p> <p>$PC = \text{vector} + 0x8$</p> <p>$CPSR \text{ mode} = SVC$</p> <p>$CPSR I = 1$ (mask 1 RA bit)</p> <p>3) MRS - Transfer the content of CPSR/SPSR to a register</p> <p>MRS $\{ \langle condn \rangle \}$ Rd, $\langle CPSR/SPSR \rangle$</p>	<p>→ 3M</p> <p>→ 2M</p>

Signature



Subject Title: MES

Subject Code: 18CS44

Question Number	Solution	Marks Allocated																				
	<p>Addressing mode are FA, FD, EA, ED</p> <p>Pre</p> <p>$r_1 = 0x02$ $r_2 = 0x03$ $SP = 0x80014$</p> <table border="1" data-bbox="845 448 1228 660"> <thead> <tr> <th>Address</th> <th>Data</th> </tr> </thead> <tbody> <tr> <td>0x80018</td> <td>0x01</td> </tr> <tr> <td>0x80014</td> <td>0x02</td> </tr> <tr> <td>0x80010</td> <td>Empty</td> </tr> <tr> <td>0x8000C</td> <td>Empty</td> </tr> </tbody> </table> <p>SP →</p> <p>Push operation</p> <p>STMFD SP!, {r1, r4}</p> <p>Post condn</p> <table border="1" data-bbox="861 806 1228 996"> <thead> <tr> <th>Address</th> <th>Data</th> </tr> </thead> <tbody> <tr> <td>0x80018</td> <td>0x01</td> </tr> <tr> <td>0x80014</td> <td>0x02</td> </tr> <tr> <td>0x80010</td> <td>0x03</td> </tr> <tr> <td>0x8000C</td> <td>0x04</td> </tr> </tbody> </table> <p>SP →</p>	Address	Data	0x80018	0x01	0x80014	0x02	0x80010	Empty	0x8000C	Empty	Address	Data	0x80018	0x01	0x80014	0x02	0x80010	0x03	0x8000C	0x04	6M
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0x80014	0x02																					
0x80010	0x03																					
0x8000C	0x04																					
3	<p>1) SWAP</p> <p>Syntax SWAP {B} [<i><condn></i>] Rd, Rm, [<i>Rn</i>]</p> <p>* Swap word between memory & register</p> <p><u>PRE</u></p> <p>mem32 [0x9000] = 0x12345678</p> <p>$r_0 = 0x00000000$ $r_1 = 0x11112222$ $r_2 = 0x00009000$</p> <p>SWAP r0, r1, [r2]</p> <p><u>POST</u> :</p> <p>mem32 [0x9000] = 0x11112222</p> <p>$r_0 = 0x12345678$ $r_1 = 0x11112222$ $r_2 = 0x00009000$</p> <p>2) SWI</p> <p>software interrupt instruction, which causes a s/w Exception</p> <p>Syntax SWI [<i><condn></i>] SWI_number.</p>	3M																				

S J C Institute of Technology
Department of Information Science and Engineering

Tutorial: III
Semester: IV

Subject: MICRO CONTROLLER AND EMBEDDED SYSTEMS (18CS44)

Section: A & B

1. Explain the characteristics of Embedded systems
2. Explain the operational and non-operational quality attributes of Embedded systems.
3. Apply the operation of Washing Machine as Application-Specific Embedded system.
And explain with the functional block diagram,
4. Explain the fundamental issues in Hardware Software co-design
5. Design & explain FSM model for automatic seat belt warning system.
6. Explain two basic approaches for designing Embedded Firmware.
7. Explain Quality attributes of embedded system?
8. With neat sketch explain various computational models in embedded system?
9. Explain the embedded Assembly language firmware development languages.
10. Explain the embedded High level language based development.
11. Explain two different approaches for building an operating system kernel.
12. Define the terms Task, Process and Threads? Explain the Process structure, process states and state transitions.
13. Explain the different types of multitasking.
14. Explain the task communication/synchronization issues
15. Explain the functional and non-functional requirements to be considered while choosing an RTOS for an Embedded design.
16. Explain basics of operating system?
17. Explain structure of process?
18. What is scheduling? Explain the various for scheduling algorithms in RTOS?
19. What is semaphore? Explain various types of semaphores in RTOS?
20. Explain integration of hardware and firmware design of embedded system.

S. Reddy



Internal Test Question paper format – 2018 Scheme

Name of the staff/s: Abdul khadar A , Sabin T T
Date: 06-08-2021

Signature:

Reviewer's Signature:

S J C Institute of Technology
Department of Information Science and Engineering

Test: III

Semester: IV Subject: MICRO CONTROLLER AND EMBEDDED SYSTEMS (18CS44)

Section: A & B

Max Marks: 50

Date: 06-08-2021

Answer the following questions

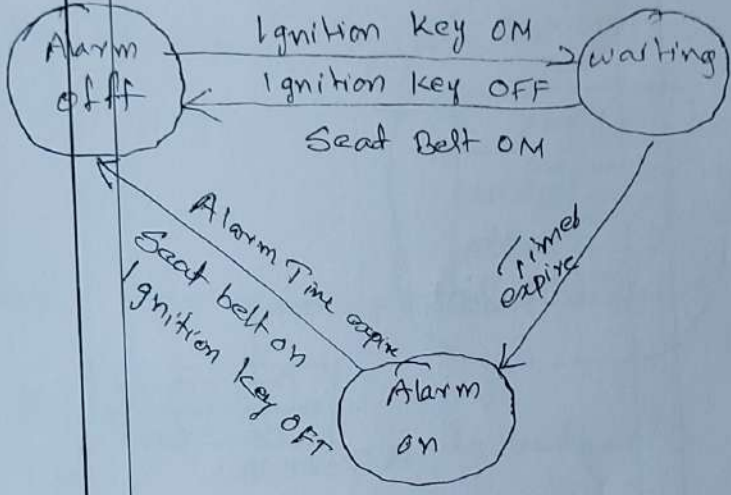
Sl.No	Questions	CO	Marks	Level
1.	Explain the characteristics of Embedded systems.	CO4	10	L2
OR				
2.	Explain the operational and non-operational quality attributes of Embedded systems.	CO4	10	L2
3.	Illustrate the operation of Washing Machine as Application-Specific Embedded system. And explain with the functional block diagram,	CO4	10	L3
OR				
4.	Illustrate the fundamental issues in Hardware Software co-design.	CO4	10	L3
5.	With neat sketch explain various computational models in embedded system?	CO4	10	L3
OR				
6.	Design & explain FSM model for automatic seat belt warning system.	CO4	10	L3
7.	Discuss the terms Task, Process and Threads? Explain the Process structure, process states and state transitions.	CO4	10	L3
OR				
8.	Illustrate the basics of operating system and need for an operating system?	CO4	10	L3
9.	Explain the task communication/synchronization issues.	CO4	10	L2
OR				
10.	Explain the functional and non-functional requirements to be considered while choosing an RTOS for an Embedded design.	CO4	10	L2



Question Number	Solution	Marks Allocated
	<p>Non-functional Requirements:</p> <ul style="list-style-type: none">① Custom developed or off the shelf② Cost③ Development and Debugging Tools Availability.④ Ease of use⑤ After sales	4 M.

S. Reddy



Question Number	Solution	Marks Allocated
6	 <p>FSM model for automatic seat belt warning system diagram</p> <p>Explanation</p> <p>Task: Defined as the program in execution and the related information maintained by the OS</p> <p>Process: is a program or part of it in execution. It is also known as instance of a program in execution</p> <p>Thread: is a single sequential flow of control within a process.</p> <p><i>[Signature]</i></p>	<p>4 M 6 M</p> <p>3x1 3 M</p>



Question Number	Solution	Marks Allocated
3	<p>Functional block diagram</p>	5M
4	<p>illustrate operation of washing machine</p> <ul style="list-style-type: none"> - Selecting the model Selecting the Architecture Selecting the language Partitioning s/w requirements into h/w and s/w <p>Explain each 4x2 1/2</p>	5M 10M
5	<ul style="list-style-type: none"> 1) Data Flow Graph/diagram 2) Data control Data flow graph. 3) state machine model 4. Sequential Program model <p>Explain with suitable diagram 4x2 1/2</p>	10M

SJR

DEPARTMENT : Information Science & Engineering

TEST-III Scheme & Solutions

18CS44

Sem : 4th.

Subject Title: Micro Controller and Embedded Systems

Question Number	Solution	Marks Allocated
1	1- Application and Domain Specific 2- Reactive and Real time 3- Operates in Harsh Environments 4- Distributed 5- Small size and weight 6- Power concerns List down characteristics Explanation of each	4M 6M.
2	Operational quality attributes 1- Response 2- Through put 3- Reliability 4- Maintainability 5- Security 6- Safety. List all the attributes Explanation Non operational quality attributes. 1) Testability & Debug-ability 2) Evolvability 3) Portability 4) Time to Prototype and market 5) Per unit and total cost Explanation	[10] 2M 3M 5x1=5 [10]

SJB

Q. 08	a	Explain the fundamental issues in Hardware Software co-design.	L1	04
	b	Design & explain FSM model for automatic seat belt warning system.	L3	06
	c	Explain two basic approaches for designing Embedded Firmware.	L2	10
Module-5				
Q. 09	a	Explain two different approaches for building an operating system kernel.	L2	06
	b	Define the terms Task, Process and Threads? Explain the Process structure, process states and state transitions.	L2	10
	c	Explain the different types of multitasking.	L1	04
OR				
Q. 10	a	Explain the task communication/synchronization issues.	L2	08
	b	Explain the functional and non-functional requirements to be considered while choosing an RTOS for an Embedded design.	L2	08
	c	Write a note on an emulator and debugging techniques.	L1	04

*Bloom's Taxonomy Level: Indicate as L1, L2, L3, L4, etc. It is also desirable to indicate the COs and POs to be attained by every bit of questions.

Model Question Paper-1 with effect from 2018-19 (CBCS Scheme)

USN

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Fourth Semester B.E. Degree Examination Microcontroller and Embedded Systems

TIME: 03 Hours

Max. Marks: 100

Note: Answer any five full question, choosing ONE full question from each module

Module -1			*Bloom's Taxonomy Level	Marks
Q.01	a	Differentiate between RISC and CISC processors.	L1	05
	b	Explain the major design rules to implement the RISC philosophy.	L2	05
	c	Explain ARM core data flow model with neat diagram.	L2	10
OR				
Q.02	a	Explain the programmer's model of ARM processors with complete register sets available.	L2	04
	b	With the help of bit layout diagram explain current program status register of ARM.	L2	06
	c	What is pipeline in ARM? Illustrate with an example. Show the pipeline stages of ARM7, ARM9 and ARM10.	L2	10
Module-2				
Q. 03	a	Write and explain arithmetic instructions with respect to the ARM processor	L2	06
	b	Discuss the load & store instructions with respect to the Single Register Transfer	L2	08
	c	Explain briefly co-processor instructions of ARM processor.	L2	06
OR				
Q.04	a	Design ARM assembly language program to perform the addition and multiplication of two 32 bit numbers.	L3	04
	b	Define instruction scheduling? Explain the rules summarizing the cycle timings for common instruction classes on the ARM9TDMI.	L2	06
	c	Explain the scheduling of following instructions with respect to the ARM9TDMI pipeline implementation, i) STR ii) LDRH iii) B Label	L3	10
Module-3				
Q. 05	a	Differentiate Embedded systems and General purpose computing systems.	L1	04
	b	What are the major application areas of Embedded systems? Explain the various purposes of embedded systems.	L2	06
	c	Explain the system core of the Embedded systems.	L2	10
OR				
Q. 06	a	Explain the interfacing of following I/O subsystems with Embedded systems i) 7-Segmnet LED Display ii) Stepper Motor.	L2	10
	b	Write a short note on onboard communication interfaces in Embedded systems	L2	06
	c	Explain the oscillator unit of the Embedded system.	L1	04
Module-4				
Q. 07	a	Explain the characteristics of Embedded systems.	L1	04
	b	Explain the operational and non-operational quality attributes of Embedded systems.	L2	06
	c	With the functional block diagram, explain the operation of Washing Machine as Application-Specific Embedded system.	L2	10
OR				

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2017-18

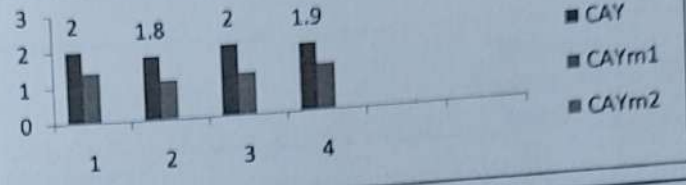


S J C INSTITUTE OF TECHNOLOGY
Chickballapur - 562 101
Department of Information Science and Engineering

Course Title	MICROPROCESSOR AND MICROCONTROLLER				Course Code	C214	
Subject Code	15CS44	Semester	4	Section	A & B	Emp.ID	1082
Faculty Name	ABDUL KHADAR A & SABIN TT				No.students	93	

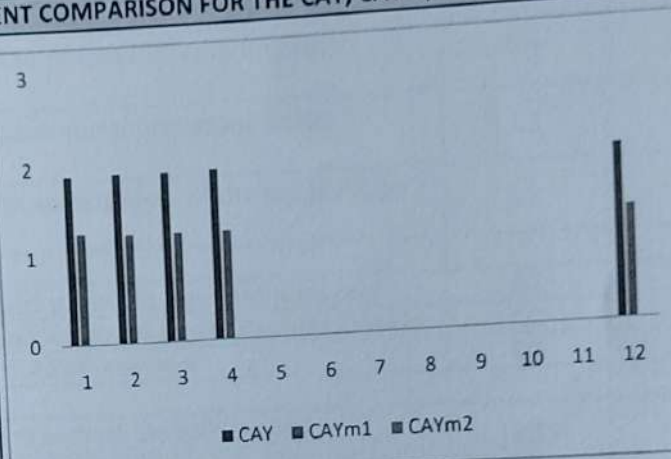
CO-ATTAINMENT COMPARISON FOR THE CAY, CAY-1, CAY-2

Sl.	CO_ID	2017-18			2016-17			2015-16		
		2017-18	2016-17	2015-16	2017-18	2016-17	2015-16	2017-18	2016-17	2015-16
1	C214.1	2	1.4							
2	C214.2	1.8	1.1							
3	C214.3	2	1.2							
4	C214.4	1.9	1.3							



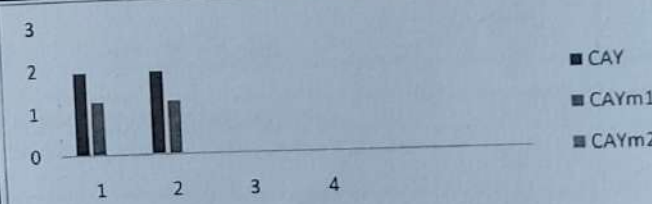
PO-ATTAINMENT COMPARISON FOR THE CAY, CAY-1, CAY-2

Sl.	PO-No.	2017-18			2016-17			2015-16		
		2017-18	2016-17	2015-16	2017-18	2016-17	2015-16	2017-18	2016-17	2015-16
1	PO-1	1.91	1.26							
2	PO-2	1.92	1.23							
3	PO-3	1.91	1.23							
4	PO-4	1.92	1.23							
5	PO-5									
6	PO-6									
7	PO-7									
8	PO-8									
9	PO-9									
10	PO-10									
11	PO-11									
12	PO-12	1.93	1.25							



PSO-ATTAINMENT COMPARISON FOR THE CAY, CAY-1, CAY-2

Sl.	PSO-No.	2017-18			2016-17			2015-16		
		2017-18	2016-17	2015-16	2017-18	2016-17	2015-16	2017-18	2016-17	2015-16
1	PSO-1	1.93	1.25							
2	PSO-2	1.94	1.26							
3	PSO-3									
4	PSO-4									



Academic Year	Course Instructor Name
2017-18	ABDUL KHADAR A & NAGESH R
2016-17	
2015-16	

Signature of Course Instructor

Signature of HOD/DAC

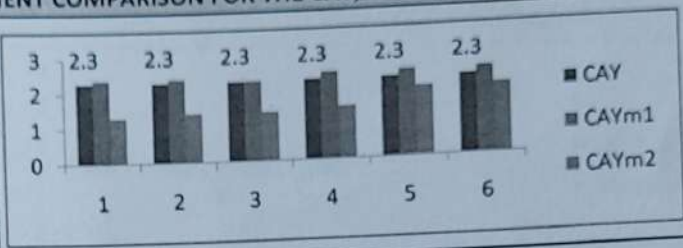
SJCIT/NBA/
S&F-REPT/
2021-22



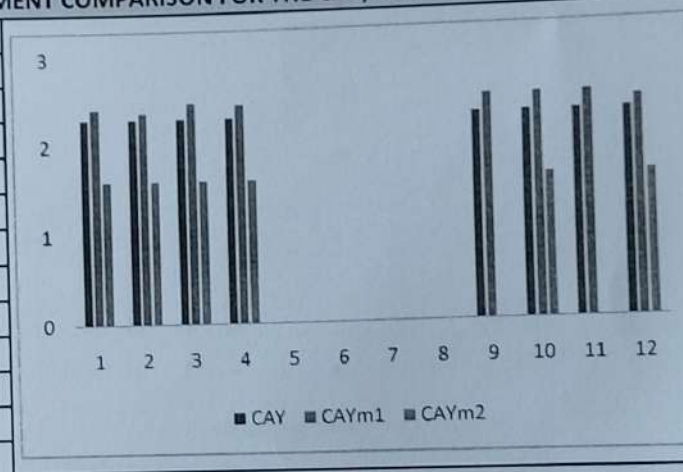
S J C INSTITUTE OF TECHNOLOGY
Chickballapur - 562 101
Department of Information Science & Engineering

Course Title	MICROPROCESSORS AND EMBEDDED SYSTEMS				Course Code	C214	
Subject Code	18CS44	Semester	4	Section	A & B	Emp.ID	1737
Faculty Name	Abdul Khadar A/Sabin T T				No.students	119	

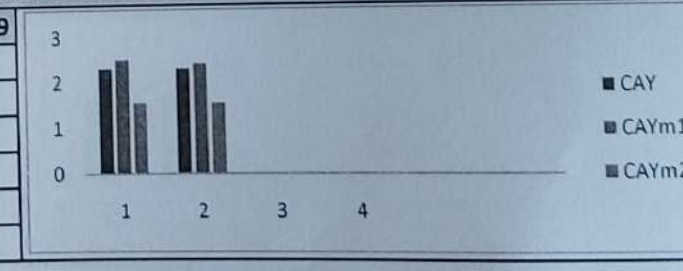
Sl.	CO_ID	CO-ATTAINMENT COMPARISON FOR THE CAY, CAY-1, CAY-2		
		2020-21	2019-20	2018-19
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2	C214.2	2.3	2.4	1.4
3	C214.3	2.3	2.3	1.4
4	C214.4	2.3	2.5	1.5
5	C214.5	2.3	2.5	2
6	C214.6	2.3	2.5	2



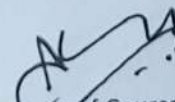
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2	PO-2	2.3	2.37	1.6
3	PO-3	2.3	2.48	1.6
4	PO-4	2.3	2.45	1.6
5	PO-5			
6	PO-6			
7	PO-7			
8	PO-8			
9	PO-9	2.3	2.5	
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11	PO-11	2.3	2.5	
12	PO-12	2.3	2.43	1.6

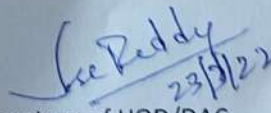


Sl.	PSO-No.	PSO-ATTAINMENT COMPARISON FOR THE CAY, CAY-1, CAY-2		
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1	PSO-1	2.3	2.5	1.55
2	PSO-2	2.3	2.41	1.55
3	PSO-3			
4	PSO-4			



Academic Year	Course Instructor Name
2020-21	Abdul Khadar A/Sabin T T
2019-20	
2018-19	


Signature of Course Instructor


Signature of HOD/DAC