Estd : 1986

||Jai Sri Gurudev||

Sri Adichunchanagiri Shikshana Trust (R.)

SJC INSTITUTE OF TECHNOLOGY

An Autonomous Institution under VTU from 2024-25

AICTE Approved, Accredited by NAAC with A+ Grade & NBA (CSE, ISE, ECE, ME, CV & AE), Gold Rated by QS I-Gauge

P.B. No.20, B.B Road, Chikkaballapur - 562 101, Karnataka

www.sjcit.ac.in

SUMMER SCHOOL TRAINING PROGRAM

ON

FPGA MODELING

FROM ALGORITHM TO HARDWARE IMPLEMENTATION

20 – 25 JULY 2026

Organized by

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

IEEE Women in Engineering

CENTRE OF EXCELLENCE VLSI & IMAGE PROCESSING

IEEE BANGALORE SECTION

IEEE Student Branch SJC Institute of Technology

INSTITUTION'S INNOVATION COUNCIL (Ministry of Education Initiative)

ABOUT THE PROGRAM

A comprehensive hands-on summer school designed to bridge the gap between digital design theory and practical FPGA hardware implementation using industry-standard tools and platforms.

KEY LEARNING OUTCOMES

- Understand FPGA Architecture and Design Flow
- Learn Verilog HDL for Hardware Design
- Design Combinational and Sequential Circuits
- Develop Finite State Machine (FSM) Based Systems
- Perform Simulation, Synthesis and Verification
- Apply Timing Analysis and Optimization Techniques
- Implement Real-Time Applications on FPGA Hardware
- Develop Hardware Accelerators and Mini Projects

PROGRAM HIGHLIGHTS

- Expert Lectures
- Hands-on FPGA Labs
- Algorithm-to-Hardware Mapping
- DSP Applications on FPGA
- FPGA Programming and Optimization
- Mini Project Development
- Industry-Oriented Learning Approach

TOOLS & PLATFORM

- Xilinx Vivado Design Suite
- Artix FPGA Development Board
- RTL Design & Verification Flow
- Hardware Debugging Techniques

TARGET PARTICIPANTS

- UG / PG Students
- Diploma Students (ECE)
- B.Sc. / M.Sc. (Electronics)

PROGRAM SCHEDULE (MAJOR TOPICS)

DAY 1 20 JUL 2026	DAY 2 21 JUL 2026	DAY 3 22 JUL 2026	DAY 4 23 JUL 2026	DAY 5 24 JUL 2026
FPGA Architecture & Verilog HDL	Combinational & Sequential Logic Design	FSM Design & FPGA Implementation	Timing Analysis, DSP & Optimization	Hardware Accelerators, Mini Project & Assessment

WHY ATTEND?

- Gain practical FPGA development skills
- Work directly on FPGA hardware boards
- Learn industry-standard design methodologies
- Build real-time digital systems
- Enhance employability in VLSI and Embedded Domains

SCAN TO REGISTER

Seats are Limited!

CONTACT

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Venue:
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SJC Institute of Technology,
Chikkaballapur – 562 101, Karnataka

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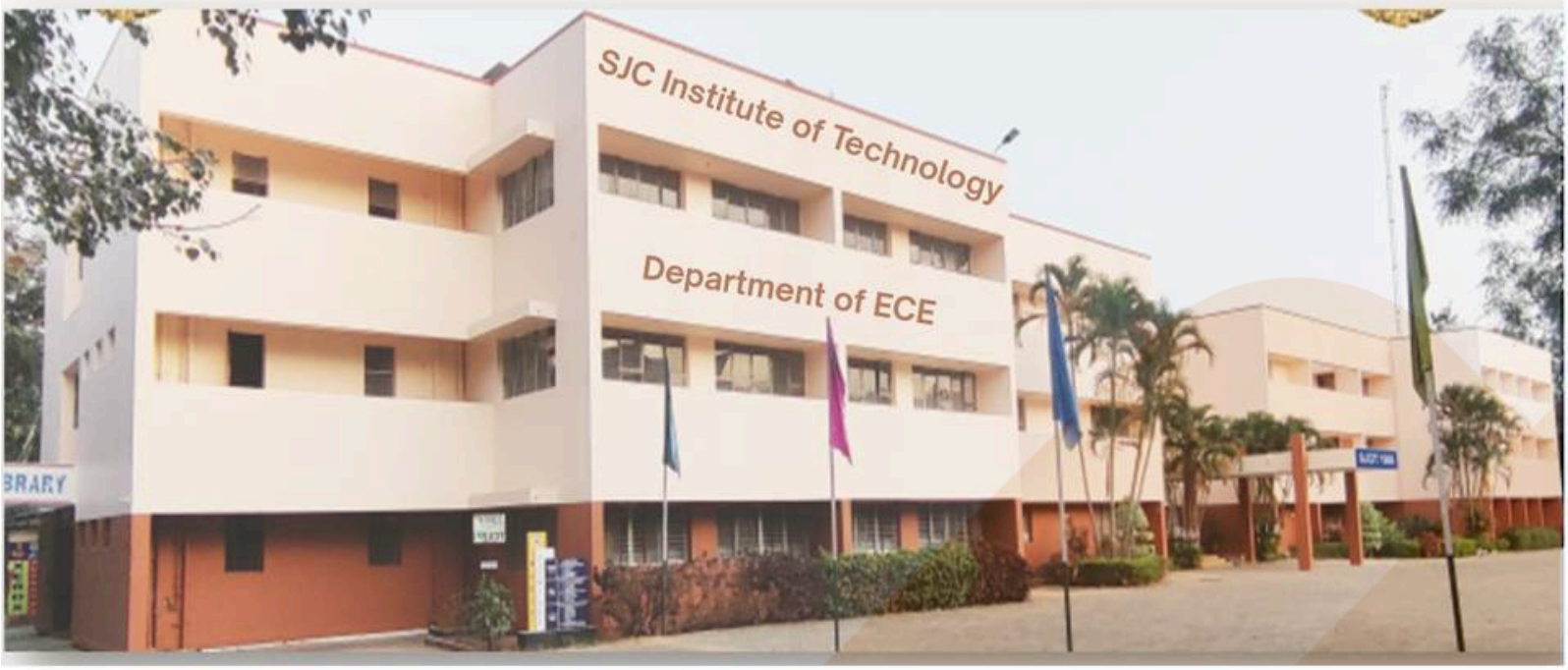
Summer School Training Program On

FPGA Modeling - From Algorithm to Hardware Implementation

In Association with
Centre of Excellance in VLSI & Image Processing

Organized by
Department of Electronics and Communication Engineering

July 20 - 25, 2026



ABOUT THE INSTITUTION

SJCIT is a premier institute established in 1986 by Sri Adichunchanagiri Shikshana Trust® by the divine soul Paramapoojya Jagadguru Padmabhushana Sri Sri Sri Dr. Balagangadharanatha Maha Swamiji. The trust is under the astute visionary & spiritual guidance of Paramapoojya Jagadguru Sri Sri Sri Dr. Nirmalanandanatha Maha Swamiji. SJCIT is one of the renowned technical institutions providing quality education in Karnataka. The Institution offers Ten UG Courses: CSE, ISE, AI-ML, AIDS, CSD, ECE, ME, CV, AE & AS and Five PG Courses in Engineering and MBA along with Nine VTU recognized R&D centers. Six UG Courses are accredited by NBA & the Institute is accredited by NAAC with "A+" Grade and has become Autonomous Institute under VTU from 2024-25

ABOUT THE ECE DEPARTMENT

The Department of Electronics & Communication Engineering established with B.E & M. Tech courses, Research & Development Centre, Centre of Excellance in IoT, Centre of Excellence in Image Processing & VLSI and Dhritvan Space Lab. The faculty and students are regularly trained in latest technological developments and believes in practical teaching methodology. The department has got well equipped state of art infrastructure required for Research & Development in the field of advanced engineering. The department has a vision to give a solid blend of practical and theoretical ideas to the students to make them highly qualified professionals; The Department is accredited by NBA.

About Summer School Program:

The main objectives of the summer school propgram are:

- **Understand fundamentals of FPGA architecture and design flow**
- **Learn Hardware Description Languages (HDL) – Verilog/VHDL**
- **Develop skills in simulation, synthesis, and timing analysis**
- **Implement real-time digital systems on FPGA boards**
- **Bridge the gap between theory and practical hardware design**

Key Concepts Covered ,Tools & Platforms:

- FPGA Architecture & Design Flow
- Combinational and Sequential Circuit Modeling
- Finite State Machine (FSM) Design
- Timing Constraints and Optimization
- RTL Design & Verification
- IP Core Integration
- Hardware Debugging Techniques
- Xilinx Vivado
- FPGA Board (ARTIX)

Outcome of the Program :

- Design and simulate digital systems using HDL
- Implement designs on FPGA hardware
- Analyze timing and optimize performance
- Develop real-time hardware-based projects

Content of Program to be covered are as follows:

- Introduction to FPGA
- HDL Fundamentals
- Combinational & Sequential Logic
- FSM Design
- Simulation & Verification
- Synthesis & Implementation
- FPGA Programming
- Advanced Topics

Target Participants

Students (UG/PG), Diploma in ECE, B.Sc/M.Sc (Electronics)

Contact Details:

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Divine Blessings

His Holiness Jagadguru Padmabhushana Sri Sri Sri Dr. Balagangadharanatha Maha Swamiji
Founder President, Sri Adichunchanagiri Shikshana Trust®

Chief Patron

His Holiness Jagadguru Sri Sri Sri Dr. Nirmalanandanatha Maha Swamiji
President, Sri Adichunchanagiri Shikshana Trust®

Patron

Poojya Sri Sri Mangalanatha Swamiji
Secretary, SAST ®, Chickballapur.

Program Chair

Dr. G T Raju
Principal, SJCIT

Finance Chair

Mr. Rangaswamy G R
Administrative Officer, SJCIT

Organizing Chair

Dr. Manjunath Kumar B H
Dean (Academics), SJCIT

Convener

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Professor & Head, ECE

Coordinator

Dr. K. Ezhilarasan,
Associate Professor, ECE

Co-Coordinators

Dr.Bhargavi S,
Professor, ECE
Dr.Veena S,
Associate Professor, ECE

Organizing Committee

Dr. Manjula K, Associate Professor, ECE
Dr. Mohan Babu C, Associate Professor, ECE
Dr. Savitha M M, Associate Professor, ECE
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Prof. Srivani E N, Assistant Professor, ECE
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Prof. Byreddy, Assistant Professor, ECE
Prof. Sahana , Assistant Professor, ECE

Technical Committee

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Dr. Manjunath S, Associate Professor, ECE
Dr. Hareesh Kumar , Associate Professor, ECE
Dr. Ravikiran R, Associate Professor, ECE
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Prof. Vishala I L, Assistant Professor, ECE
Prof. Anitha C, Assistant Professor, ECE
Prof. Manjesh N, Assistant Professor, ECE
Prof. Harish T L, Assistant Professor, ECE
Prof. Gowthami, Assistant Professor, ECE

Program Schedule

Time	Day 1 (20 Jul 2026)	Day 2 (21 Jul 2026)	Day 3 (22 Jul 2026)	Day 4 (23 Jul 2026)	Day 5 (24 Jul 2026)
09:00 – 09:30 AM	Registration & Inauguration	Recap of Day 1	Recap of Day 2	Recap of Day 3	Recap of Day 4
09:30 – 11:00 AM	FPGA Architecture and Design Flow	Combinational Logic Design using Verilog HDL	Finite State Machine (FSM) Design Concepts	Timing Analysis and FPGA Optimization Techniques	Algorithm-to-Hardware Mapping Methodology
11:00 – 11:15 AM	**Tea Break**	**Tea Break**	**Tea Break**	**Tea Break**	**Tea Break**
11:15 – 12:15 PM	Introduction to Verilog HDL	Sequential Circuit Design and Modeling	FSM-Based Controller Design	Pipelining and Parallel Processing in FPGA	Hardware Accelerator Design Concepts
12:15 – 1:15 PM	HDL Coding Guidelines and Best Practices	Simulation and Testbench Development	Synthesis and Implementation Flow	DSP Applications on FPGA	Case Studies in FPGA-Based System Design
1:15 – 02:00 PM	**Lunch Break**	**Lunch Break**	**Lunch Break**	**Lunch Break**	**Lunch Break**
02:00 – 03:00 PM	Hands-on Session: FPGA Tool Setup and Basic Design	Hands-on: Design and Simulation of Digital Circuits	Hands-on: FSM Implementation on FPGA	Hands-on: Digital Signal Processing Design	Mini Project Development
03.00 - 03.15 PM	**Tea Break**	**Tea Break**	**Tea Break**	**Tea Break**	**Tea Break**
03:15 – 04:00 PM	Hands-on: LED, Switch and Seven-Segment Interfacing	Hands-on: Counters and Registers	Hands-on: Traffic Light Controller Design	Hands-on: FIR Filter/PWM Generator Design Q&A and Assessment	Mini Project Implementation, Feedback & Valedictory